Hybrid Silicon Photonic Circuits and Transceiver for 50 Gb/s NRZ Transmission Over Single-Mode Fiber

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(Invited Paper)

***Abstract*—This paper presents a 50 Gb/s per lane hybrid BiCMOS and silicon photonic integrated circuit for use in fiber optic communications. Fine pitch copper pillars are used to integrate electronics and silicon photonics. The resulting device demonstrates the generation and detection of up to 56 Gb/s NRZ optical signals over 2-km standard single-mode fiber at 1310-nm wavelength. At 40 Gb/s, the link operates error free, and at 56 Gb/s well below KR4 RS-FEC operating BER. The power dissipation of TX including CW laser is 600 mW (450-mW driver, 150-mW CW laser), RX is 150 mW, resulting in total per channel of less than 750 mW.**

***Index Terms*—50 Gb/s, Mach–Zehnder modulator, silicon photonics.**

I. Introduction

AFTER more than a decade of research and investment into silicon photonic devices [1], [2], and many debates over the merits [3], [4], the last few years have seen the start of broad based commercial development of silicon photonics for Telecom, Datacom, High Performance Computing and chip-to-chip interconnect applications. This is motivated by the promise of large scale photonic integration, low-cost high-yield manufacturing, and inherent reliability, levering the huge investment into complementary metal-oxide semiconductors (CMOS). While there are only a few silicon photonics products in the market, the availability of mature silicon photonics foundries and established development infrastructure, including computer aided design tools, IP blocks, and multi-project-wafers [5], is set to transform the optics industry by enabling fabless development model successfully used for integrated circuits (IC) development.

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Today at rates up to 28 Gb/s, silicon photonics competes against mature III–V semiconductor technologies like directly modulated laser (VCSEL and DFB laser) and electro-absorption modulator laser (EML). Directly modulated lasers can be pushed to higher data rates by use of transmit and receive equalization but at the cost of higher power dissipation. Silicon photonic devices have the potential for faster speed without a power dissipation increase enabling high-density next generation 100 and 400 Gb/s Ethernet interfaces [6]. Silicon photonics 50 Gb/s transmit and receive devices have been reported [7], however these rely upon large swing Mach–Zehnder drivers, commercial TIAs, and 50 Ω environment resulting in high power. Furthermore, the transmit power dissipation is often only reported for the modulator and does not include the continuous wave (CW) laser source.

This paper describes a fully integrated 2 channel 40 to 56 Gb/s NRZ 1310 nm duplex single mode fiber (SMF) optical link using transmit and receive optical devices in STMicroelectronics PIC25G silicon photonics technology. The silicon photonic device is packaged in a CFP4 transceiver. The reported 750 mW per channel delivers on the silicon photonics promise of higher lane rate without increase in power dissipation.

II. Background

Historically, Telecom data rates increased in steps of 4×, for example 2.5 to 10 to 40 Gb/s. Ethernet (Datacom) data rates increased in steps of 10×, for example 1 to 10 to 100 Gb/s. During standardization of 100 Gb/s these trends changed. Telecom rate aligned with Ethernet rate so that highest speed Ethernet could be transported efficiently; the Telecom step after 40 Gb/s was 100 Gb/s. Data rate increments decreased to 2×, including standardization of lower rates to fill in missing steps, for example 25 Gb/s Ethernet. This is driven by desire to cost optimize interfaces by matching data rates to technology lane rates.

Historically, technology lane rates, including of ICs like SerDes, increased in steps of 2× or nearly 2×, for example 1 to 2.5 to 5 to 10 to 25 Gb/s. The industry is now working on 50 Gb/s as the next technology lane rate. OIF CEI-56G Project and IEEE 802.3 400G Ethernet Task Force are standardizing 50 Gb/s per lane electrical interfaces. The IEEE is considering standardizing 8 × 50 Gb/s wavelength division multiplexing (WDM) as the architecture for 400 Gb/s duplex SMF optical interface. There is also a consensus in the Datacom industry that 50 Gb/s Ethernet and 50 Gb/s per lane interfaces will be

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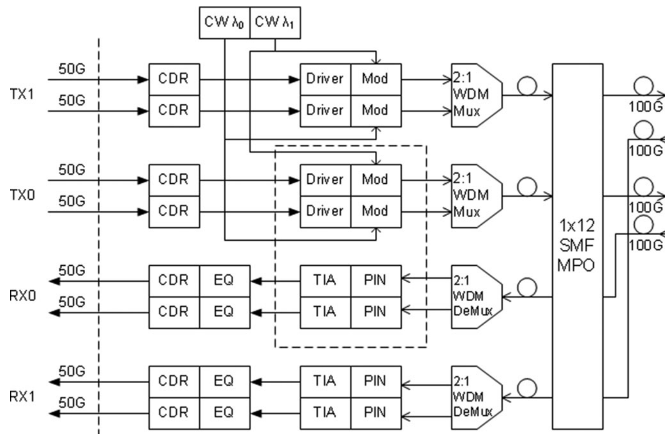

Fig. 1. 200 G transceiver block diagram example.

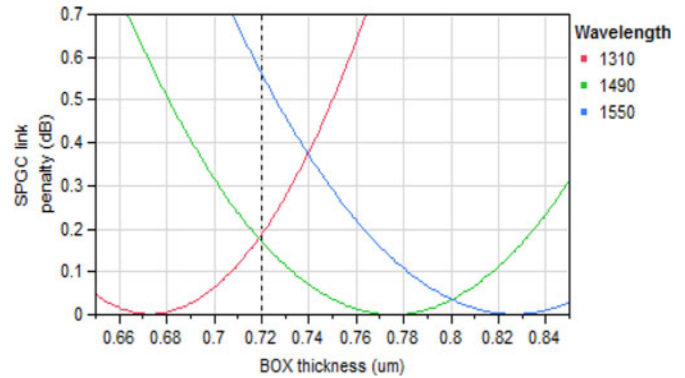

Fig. 2. Optimization of the BOX thickness for multi-wavelength applications.

standardized in a future IEEE project to support servers and high radix switches.

Today's 100 Gb/s interfaces are based on 4×25 Gb/s architecture. Future 100 Gb/s interfaces will be based on 2×50 Gb/s architecture, reducing cost and power by a factor of $2\times$ and doubling 100 Gb/s port density. Example architecture is shown in Fig. 1. The electrical interface is four lanes, which is found on popular transceivers like CFP4 and QSFP28. Two 100 Gb/s channels are supported since each lane is 50 Gb/s, resulting in total transceiver bandwidth of 200 Gb/s. Each 100 Gb/s channel is two 50 Gb/s wavelengths multiplexed on one SMF pair. Each CW laser output drives two 50 Gb/s modulators reducing per channel cost. A high density MPO connector supports multiple SMF pairs in one transceiver.

The 50G building blocks in Fig. 1 support other transceiver configurations.

One TX and RX 50G lane and one CW wavelength support one 50G optical interface over one SMF pairs.

Four TX and RX 50G lanes with no WDM Mux and DeMux and one CW wavelength support four 50G optical interfaces over four SMF pairs.

Four TX and RX 50G lanes with one 4:1 WDM Mux and 1:4 WDM DeMux and four CW wavelengths support a single 200G optical interface over one SMF pair.

Eight TX and RX 50G lanes with one 8:1 WDM Mux and 1:8 WDM DeMux and eight CW wavelengths support a single 400G optical interface over one SMF pair.

The two lane 50G TX and RX IC and Silicon photonics IC reported in this paper is shown enclosed by dashed lines in Fig. 1.

III. Process Technology for Silicon Photonics

A. Process Description

STMicroelectronics silicon photonics platform (PIC25G) [8] uses 300 mm SOI substrates with 310 nm silicon thickness on 720 nm thick buried oxide (BOX). The BOX thickness is optimized to minimize insertion loss of grating couplers [9] at both 1310 and 1490 nm. Fig. 2 illustrates Single Polarization Grating Coupler (SPGC) relative insertion loss penalty (sum of fiber and laser SPGC insertion losses minus the losses obtained using an optimal BOX thickness). The optimal BOX thickness depends on both wavelength and beam angle since the minimum grating coupler insertion loss is achieved through a constructive interference between directly scattered light and light reflected from BOX-handle interface.

Starting from this substrate material, the SOI layer is patterned in two steps. A first 193 nm lithography step, featuring a minimum space of 80 nm, is used to define the optical passive devices such as surface grating couplers (see Fig. 3(a)), splitters, waveguides and bends, and is followed by a partial Si etch. The average remaining silicon thickness after this etching step is 166 nm. The etched area defines both the slab of rib waveguides (that are used as basic element of all optical devices in the technology) and the trench depth of the grating couplers. The resulting waveguides are 0.32 μm wide with 306 nm of top SOI thickness (see Fig. 3(b)). The bend radius for such SOI thickness, slab thickness and waveguide width is about 40 μm. An 80 nm minimum trench width together with an 8 nm control of the within-wafer depth is achieved [10], allowing to reduce insertion loss and peak wavelength dispersion on both SPGC and polarization splitting grating couplers (PSGC). The second etching step consists into a full etching of silicon down to the BOX in order to realize an optical isolation between components. Trenches filling with silicon-dioxide and planarization are then performed in order to define the lateral cladding of the waveguides.

Once the optical passive components are defined, the high speed phase modulators (HSPM) based on p-n junctions are built using several steps of ion implantations. Then a SiO_2 and a SiN protection layers are deposited and opened locally to form a $CoSi_2$ silicide that is used to minimize the modulator contacts resistance. After this step, silicide is covered by a SiN layer that will be used later in the flow as a contact etch-stop-layer, and by a SiO_2 hardmask layer. Waveguide integrated high speed photo diodes (HSPD) are realized using a selective epitaxial growth of Germanium inside cavities defined in Silicon waveguides and patterned through the above mentioned SiN/SiO_2 stacked layers. The photodiode device is based on a p-i-n diode defined by ion implantations of B and P. After a 0.5 μm thick oxide deposition, TiN/W contact plugs are patterned in a single step for both HSPM and HSPD. Cross-section made using transmission electron microscopy of both HSPD and HSPM are shown in Fig. 3(c)

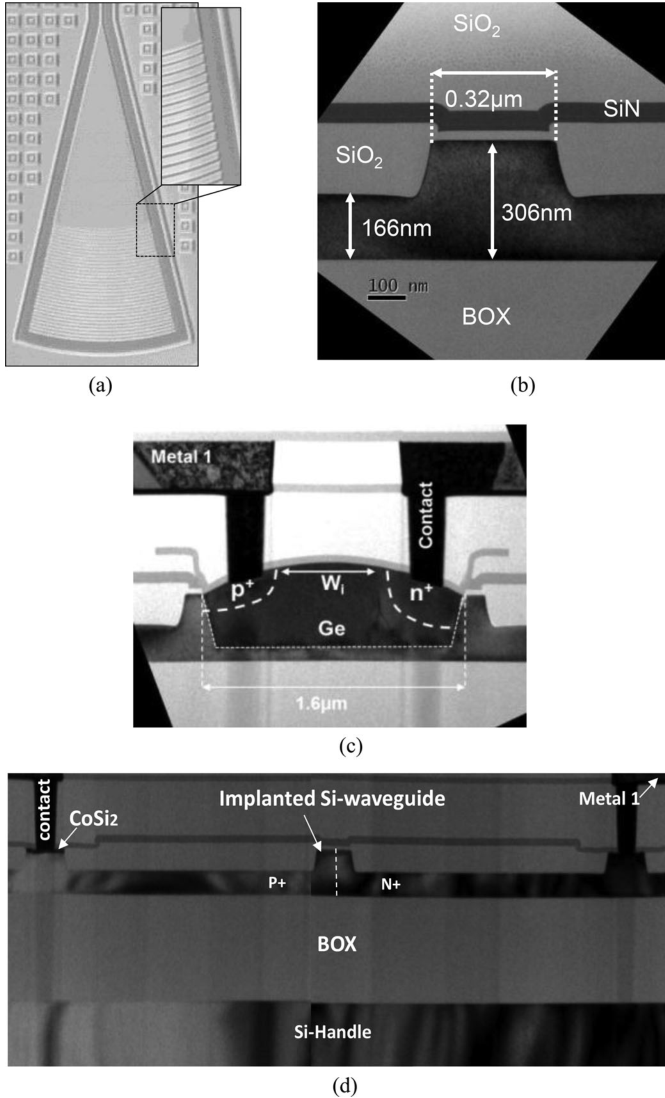

Fig. 3. (a) SEM top view of SPGC, (b) SEM cross-section of SM Rib waveguide, (c) high speed waveguide Ge photodetector (d) and integrated P/N junction depletion mode HSPM (d).

and (d). Finally four copper metal layers for interconnection and thick aluminum for wire bonding are realized.

Top view and cross-section SEM of main optical device are shown on Fig. 3. The SiN layers above the waveguide are resulting from the process steps described above.

B. Device Measurement Results

Typical performances of 1310 nm device at 50 °C are summarized in Table I.

C. Devices Improvements

Second generation of HSPM has been developed to improve performances. Based on new design and new doping levels for the N & P implants, phase shift at 2.5 V has been increased to 18°/mm, while static loss at 0 V increased from 4.2 dB/cm (first generation of HSPM) to 6 dB/cm [10].

TABLE I
PERFORMANCES AT $T = 50°$ OF 1310 NM OPTICAL DEVICE

Device	Parameter	Typical value as reported in [8] and [10]
SPGC	Peak loss (dB)	2.15
PSGC	Peak loss (dB)	3.8
Single mode waveguide	Loss (dB/cm)	1.6
Multimode waveguide	Loss (dB/cm)	0.17
HSPM	Phase shift at 2.5 V (°/mm)	10.5
	Static loss at 0 V (dB/cm)	4.2
	Cut-off frequency (GHz)	45
HSPD	Dark current at 1 V (nA)	100
	Responsivity at 1 V (A/W)	1
	Electrical bandwidth at 1 V (GHz)	>20

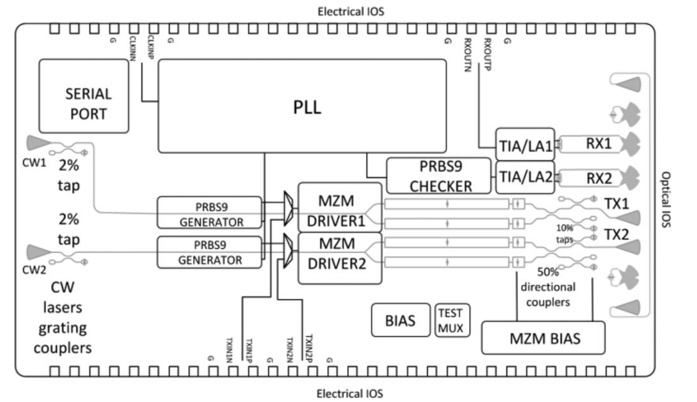

Fig. 4. EIC and PIC block diagram.

IV. SILICON PHOTONICS HYBRID IC OVERVIEW

A block diagram of the IC is shown Fig. 4. The 3-D IC consists of two face to face stacked ICs connected with fine pitch copper pillars (μ-Cu-pillars) with 20 μm diameter, 40 μm pitch and less than 10 fF and 10 pH parasitic capacitance and inductance [11]. Such low parasitic inductance and capacitance do not limit the receiver and transmitter performance of our device. The silicon photonic IC (PIC) includes all photonic passive and active devices as well as some native passive devices such as resistors and capacitors used for the modulator electrodes termination and supply decoupling.

The electronic IC (EIC) is implemented in a 0.13 μm SiGe BiCMOS technology targeting millimeter-wave and optical communication applications with high speed NPN transistors with f_t and f_{max} both exceeding 200 GHz and 1.6 V BVCEO. This technology is well suited for high voltage swing modulator drivers and trans-impedance amplifiers operating beyond 40 Gb/s. As a comparison, deep submicron 32 nm n-MOS exhibits similar f_t and f_{max} performance but the bipolar devices offer a better trade-off between voltage breakdown and cut-off frequencies when compared to CMOS.

Optical signals (SMF array and CW lasers) are vertically coupled to the PIC via grating couplers described earlier. Two types of gratings are used. One-dimensional SPGCs are used on the transmitter's outputs and CW laser input. Two-dimensional

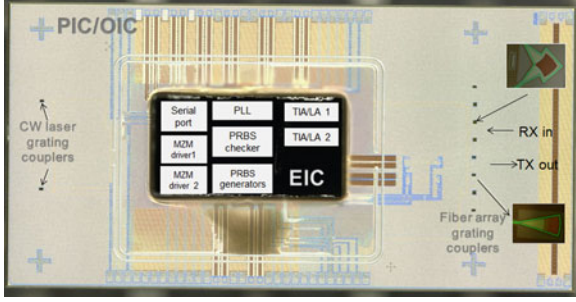

Fig. 5. Three-dimensional IC photograph.

PSGC are used on the receivers input. SPGC have approximately 2 dB insertion loss and 20 nm 1 dB bandwidth around the 1310 nm peak wavelength. PSGC have approximately 4 dB insertion loss and 20 nm 1 dB bandwidth around the 1310 nm peak wavelength. Measured PDL is below 0.5 dB with the fiber array properly aligned to the fiber grating array.

The IC includes two 56 Gb/s traveling wave electrodes (TWE) Mach–Zehnder modulator (MZM), two MZM drivers, MZM bias circuit and two 56 Gbs/ receivers consisting of high speed waveguide Ge photodetectors, TIAs and limiting amplifiers.

In order to evaluate operation above 50 Gb/s, the EIC was built with on-chip PRBS testing capability. The transmitters have two independent PRBS $2^9 - 1$ generators. One receiver output is connected to an internal PRBS $2^9 - 1$ checker. The internal PLL clock connecting the PRBS circuits enables 16 to 60 Gb/s testing capability.

The 4×8 mm IC heterogeneous silicon technologies 3-D IC die photograph is shown in Fig. 5. The electronics only represents a small fraction of the total IC area (approximately 10%) and clearly demonstrates the advantage of hybrid integration compared to a monolithic approach not only for performance but also for cost reasons. The photonic active devices footprint is also very small. The PIC die size is mostly dictated by the required area and clearance of the fiber array and CW laser coupling as well as the wire bonding pads. Finally, it is important to note that the die size does not scale linearly with the number of Tx/Rx channels. We estimate that doubling the channel count may only result in a 30% increase in die size. This highlights one of the potential advantages of silicon photonics over traditional approaches for large parallel channels counts.

V. TWE MZM Design

A. TWE Design

The PN junction carrier depletion HSPM used in the MZM exhibits a 10.5°/mm phase shift under 2.5 V bias which is equivalent to $V_\pi \cdot L = 4.3$ V·cm and a low insertion loss $\propto_{\rm optical}$ of 0.42 dB/mm. This corresponds to a 18 V·dB $V_\pi \cdot L. \propto_{\rm optical}$ figure of merit (FOM) [12].

The MZI voltage to optical power transfer is:

$$P_0(t) = \frac{P_i}{2}\left(1+\cos\left(\frac{\Delta V(t)}{V_{\pi \rm mzm}}\pi\right)\right)e^{-\alpha_{\rm optical}\cdot L_{\rm mod}} \quad (1)$$

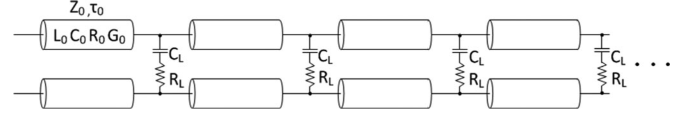

Fig. 6. Loaded transmission lines.

where P_0 and $P_{\rm i}$ are the modulator output and input optical power, $V_{\pi \rm mzm} = (V_\pi.L)/{\rm L_{mod}}$, $L_{\rm mod}$ the modulator length and $\Delta V = V_{\rm arm1} - V_{\rm arm2}$ the modulator differential voltage.

Using the equation above, maximum optical modulation amplitude (OMA) is achieved at $\pi/2$ bias point on the transfer curve for a 6–7 mm long modulator. With a 10 dBm CW laser source, modulator driver differential pk–pk drive $\Delta V = 4$ V and device performance as listed Table I, 0 dBm OMA can be achieved.

Unfortunately, the lumped electrodes model is not valid for long electrodes and for speeds of 40 Gb/s and above because the optical phase velocity of the optical signal inside the silicon waveguide is approximately 11.4 ps/mm. TWE or distributed driver architectures (or a combination of both) are traditionally used.

In order to achieve maximum electro-optical bandwidth, the velocities of the electrical driving signal and optical wave must be matched. By periodically loading transmission line electrodes (Z_0, τ_0), with PN carrier depletion phase modulator sections, the loaded transmission line transmission characteristics $(Z_{\rm loaded}, \tau_{\rm loaded})$, are altered:

$$Z_0 = \sqrt{\frac{L_0}{C_0}}, \qquad \tau_0 = \sqrt{L_0.C_0} \quad (2)$$

with Z_0 the impedance, L_0 the inductance and C_0 the capacitance per unit length and τ_0 the propagation delay ~ 6.4 ps/mm of the unloaded electrodes

$$\begin{aligned} Z_{\rm loaded} &= \sqrt{\frac{L_0}{C_0 + C_{\rm load}}} \\ \tau_{\rm loaded} &= \sqrt{L_0 \cdot (C_0 + C_{\rm load})} \end{aligned} \quad (3)$$

with $Z_{\rm loaded}$ the impedance, $C_{\rm load}$ the HSPM modulator capacitance per unit length loading the transmission line, $\tau_{\rm loaded}$ the propagation delay $\sim$11.4 ps/mm (to match the optical signal) of the loaded electrodes.

Modulator capacitance is approximately 220 fF/mm at 2 V reverse bias with a series resistance of $\sim$10 $\Omega \cdot$mm. For RF electrical and optical waves velocity matching, the TWE unloaded electrodes are 35 Ω and the loaded electrodes 20 Ω for a differential drive as shown Fig. 6.

Taking R_0 (transmission line loss, skin effect) and $R_{\rm L}$ (PN diode series resistance) into account, the loaded TWE $\gamma_{RF} = \alpha_{RF} + j\beta_{RF}$ complex propagation parameter can be expressed as:

$$\begin{aligned} \gamma_{RF} &= \sqrt{(R_0 + j\omega L_0)\cdot(G_T + j\omega\,(C_0 + C_T))} \\ \text{with}\ \ C_T &= \frac{2C_L}{1 + R_L^2 C_L^2 \omega^2}, \\ \frac{1}{G_T} &= \frac{R_L}{2}\left(1 + \frac{1}{R_L^2 C_L^2 \omega^2}\right). \end{aligned} \quad (4)$$

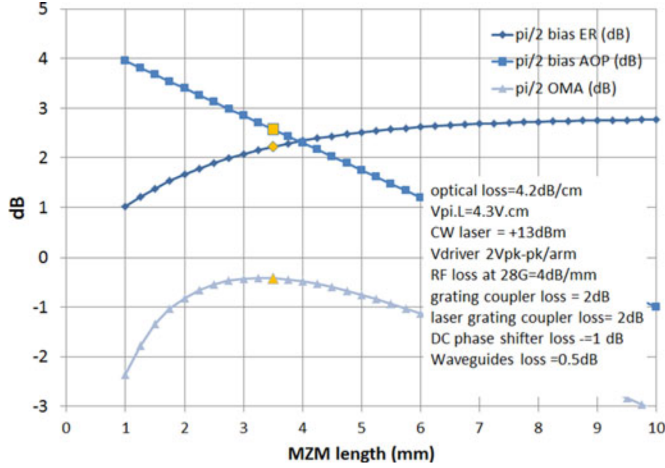

Fig. 7. Transmitter extinction ratio, average optical power and OMA versus modulator length.

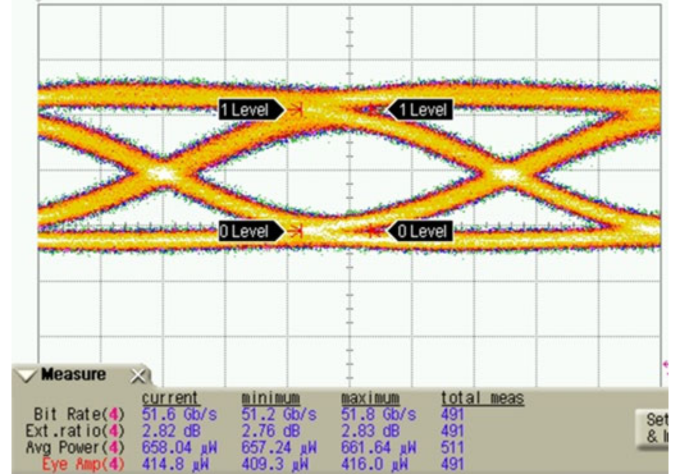

Fig. 8. 51.6 Gb/s TX eye diagram.

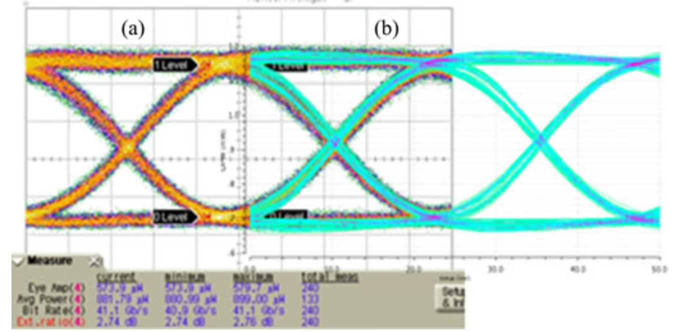

Fig. 9. 40 Gb/s, PRBS9 TX optical eye diagram at $\pi/2$ bias (a) measurement, (b) simulation.

The calculated TWE α_{RF} RF loss shows that the transmission line skin loss dominates below 28 GHz and modulator loss above 28 GHz. RF loss at 28 GHz is ~4 dB/mm. Evidently, both modulator access resistance and skin loss have to be minimized to achieve large bandwidth. Unfortunately, these parameters are, for the most part, set by the technology and on chip transmission lines. Therefore, transmitter equalization has to be provided by the driver to extend the bandwidth of the modulator.

The total amount of phase shift at the end of the two MZM arms is the cumulative phase shift of all the modulator sections along the two arms and can be calculated by integrating the voltage drive along the TWE. We find that the MZM insertion loss caused by RF losses at a given frequency is:

$$\frac{\left(1 - e^{-\alpha_{RF}(f)L_{\mathrm{mod}}}\right)}{\alpha_{RF}(f)L_{\mathrm{mod}}}. \tag{5}$$

At high frequencies, as the TWE losses caused by skin loss and the modulator access resistance become significant, increasing the length of the modulator no longer produces additional phase shift and the efficiency of the modulator does not improve.

Taking this into account, for $\alpha_{RF}(28\ \mathrm{GHz}) = 4\ \mathrm{dB/mm}$, a maximum OMA of approximately 0 dBm is achieved at $\pi/2$ bias point on the MZM transfer curve with a 13 dBm CW laser source, modulator driver differential pk–pk drive $\Delta V = 4$ V and device performance as listed Table I and ~3.5 mm long modulator as shown Fig. 7.

The PIC MZM TWE chosen length is 3.36 mm and composed of 12 $\times$ 280 μm modulator sections. The 35 Ω transmission lines are 6 μm metal4 over metal1 microstrips. The driver is ac coupled to the HSPM anodes to provide de-emphasis of the low frequencies where skin loss dominates and dc coupled on the cathode side to provide the broadband modulation. Reverse bias of 2 V is provided by the driver. The driver circuit delivers 2 V pk–pk/arm. TWE skin loss equalization required for 50 Gb/s transmission is achieved by the zero-pole compensation response of the ac coupled anode and the TWE ac termination integrated on-chip. Automatic MZM biasing circuitry sets the MZM to maximum OMA.

The second generation high speed modulator $V_{\pi} \cdot L. \propto_{\mathrm{optical}}$ FOM is 14.4 V $\cdot$ dB ($V_{\pi} \cdot L = 2.4$ V $\cdot$ cm and insertion loss $\propto_{\mathrm{optical}} = 0.6$ dB/mm) which represents a significant improvement over the modulator used in our IC. This new modulator, used with the same MZM design is expected to improve the OMA to +2 dBm and extinction ratio to about 4.8 dB using the same CW 13 dBm laser power and identical grating couplers.

B. Measurements Results

TX eye diagrams are captured using the internal PRBS generator driving the MZM driver. 51.6 Gb/s TX eye diagram is shown Fig. 8.

Transmitter optical eye diagrams lab measurements show an excellent correlation between simulation and measurement. This is illustrated in Fig. 9 and Fig. 10. Extinction ratio measured at $\pi/2$ bias point is 2.7 dB with good repeatability across multiple devices. Measured OMA was between –4 and –1 dBm. This is lower than expected. The CW laser coupling measurements show about 2 dB discrepancy between measured data and expectation. This is being further investigated.

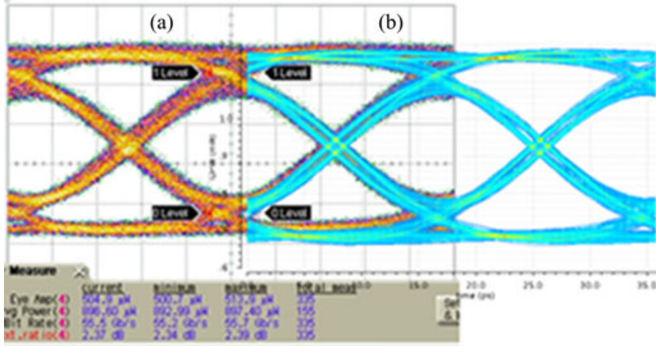

Fig. 10. 56 Gb/s, PRBS9 optical TX eye diagram at $\pi/2$ bias (a) measurement, (b) simulation.

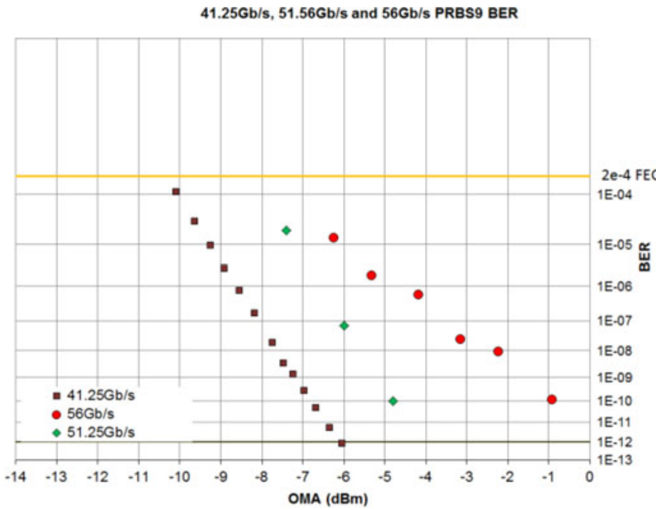

Fig. 11. Receiver BER versus OMA using the on-chip PRBS checker, 41.25, 51.56 and 56 Gb/s.

VI. TIA and Waveguide Germanium Photodetector Receiver

A. Design

Waveguide Ge photodetectors integrated with small silicon waveguides exhibit very low capacitance and do not suffer the bandwidth/responsivity trade-off found in surface illuminated p-i-n photodetectors. Because waveguide PD devices capacitance can be one to two order of magnitude lower than vertical p-i-n PDs, the input referred noise of the TIA can be greatly reduced. The advantage becomes even more apparent looking at the input-referred noise current spectral density main contributors [13]. The f^2 high frequency noise component contributed by the TIA input transistor peaks at higher frequencies. For a BiCMOS TIA, the input SiGe HBT base resistance thermal noise and collector shot noise can be lowered to a level where the TIA input stage gain resistor (feedback resistor in a shunt-feedback TIA or collector resistor in a common base TIA) becomes the main contributor.

Unfortunately, the peak insertion loss caused by the PSGC is around 4 dB and is high enough to overcome the sensitivity improvement expected from the waveguide PD.

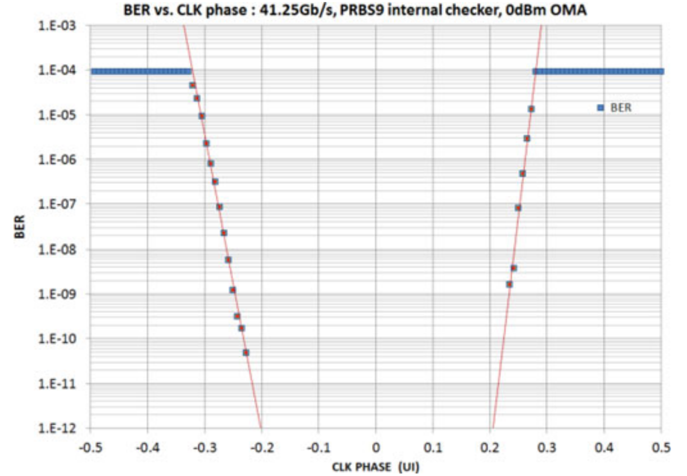

Fig. 12. Receiver BER versus decision circuit clock phase.

This design uses a differential common base topology with both PD anodes and cathodes dc coupled to the TIA differential input. The TIA provides 1.8 V reverse bias to the photodetector. TIA expected input referred noise is 3.5 μA RMS and bandwidth is 38 GHz.

B. Measurement Results

Measured PRBS9 receiver OMA sensitivity at 10^{-12} BER and 40 Gb/s is –6 dBm. BER vs. OMA for 41.25Gb/s, 51.56Gb/s and 56Gb/s using the internal PRBS checker is shown Fig 11. PRBS31 was also measured using a 40G commercial IC included in the CFP4 transceiver. PRBS31 OMA sensitivity at 10^{-12} BER and 40 Gb/s is –5.3 dBm. 56 Gb/s receiver OMA sensitivity at 10^{-5} BER is below –6dBm.

The internal PRBS checker decision circuit clock phase can be swept to cover one UI as shown Fig. 12. At 0 dBm OMA, the eye opening at 1e–12 BER exceeds 0.4UI.

C. IC Power Dissipation

The total power dissipation per lane is 750 mW and includes the MZM driver, CW laser, TIA and limiting amplifier. This corresponds to 18 pJ/bit for 41 Gb/s and 14 pJ/bit for 56 Gb/s transmission. Circuits contributions are depicted Fig. 13.

VII. Other Applications

In addition to increasing lane rate and number of lanes to increase the data rate, the industry is also studying increasing the number of bits per baud, i.e., higher order modulation. An approach that increases rate by 2× and is well suited to SiP PIC implementation is PAM-4 (Pulse Amplitude Modulation), which encodes two bits into four intensity levels. The topology could use two cascaded binary weighted MZMs driven by the LSB and MSB of the two bit symbol for instance. Similar techniques and technology as reported in this paper for 56 Gb/s NRZ, results in good 28 GBaud PAM-4 (56 Gb/s) performance.

Fig. 14 shows a simulated 28 GBaud PAM-4 (56 Gb/s) transmitter eye at room temperature and typical process.

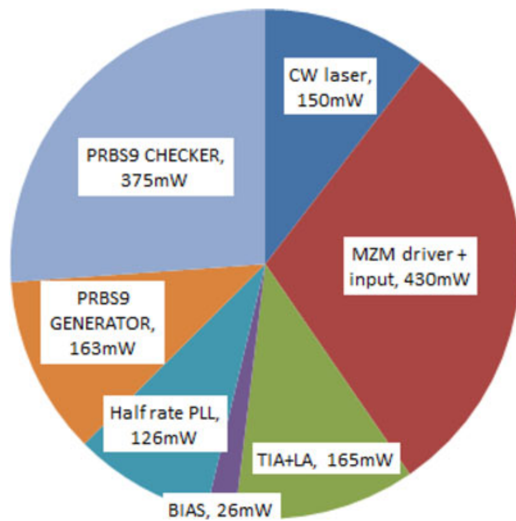

Fig. 13. IC power dissipation.

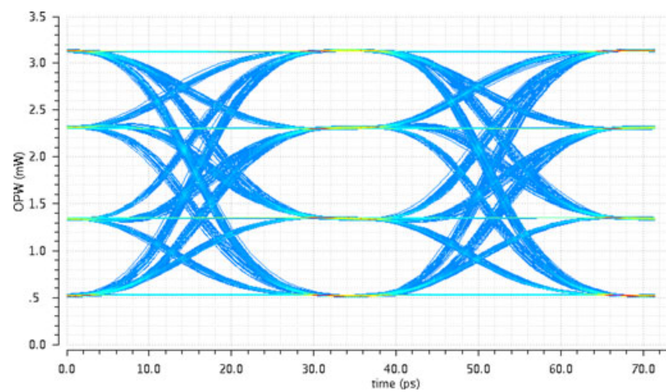

Fig. 14. Simulated 28 GBaud PAM-4 (56 Gb/s) TX eye.

Transmission over 2 km of standard SMF does not significantly degrade the eye and enables simple receiver and equalizer architecture.

VIII. Conclusion

This paper describes NRZ transmit and receive silicon photonics operating from 40 to 56 Gb/s, integrated into a first reported 112 Gb/s (2 × 56 Gb/s) optical transceiver. Future work will focus on reducing insertion losses, improving transmitter extinction ratio, and integrating WDM components. The technology is also applicable to 28 GBaud higher order modulation like PAM-4.

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