Vertical Line Card (VLC)

Advanced Technologies for Line Card Design Panel

Track 07: Optimizing High-Speed Link Design

1 February 2023, 12:30 - 1:30 PM PT

DesignCon® 2023

WHERE THE CHIP MEETS THE BOARD

Santa Clara, California

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Update to ECOC 2022 Tu3C.2 presentation, Datacenter Optical Transceivers in the Next Decade, C. Cole, et al.

Outline

➢ Introduction

- Dual Front ASIC VLC Baseline
- Vertical OSFP Connector
- Vertical OSFP-XD Connector
- Stripline vs. Twinax Loss
- Single Front ASIC VLC Alternatives
- Conclusions
- Appendix 1: PCIe
- Appendix 2: Vertical OSFP Connector FEXT & NEXT
- Appendix 3: Vertical OSFP-XD Connector FEXT & NEXT
- Appendix 4: Rack Power Limitations

Abstract

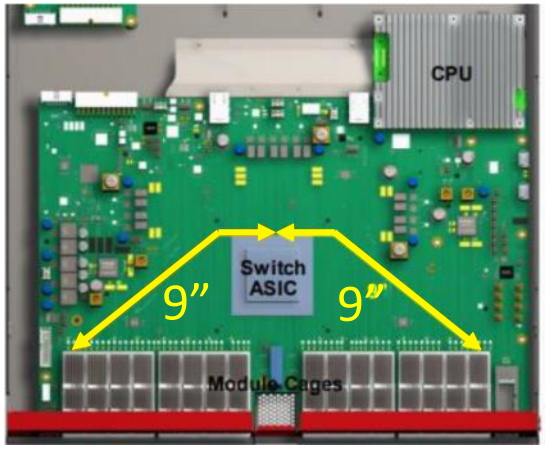
The traditional horizontal line card (HLC) technology with front pluggable optics and PCB trace interconnect to the ASIC has served the industry well. However, as electrical signaling rates have increased, the signal integrity has been degraded because of the PCB trace length and right-angle connector geometry. Industry is developing three advanced technologies to solve this challenge: 1) twinax-over-PCB, 2) near package optics (NPO), and 3) vertical line card (VLC). The panelists will present the technical details and challenges of each approach and debate their relative merits.

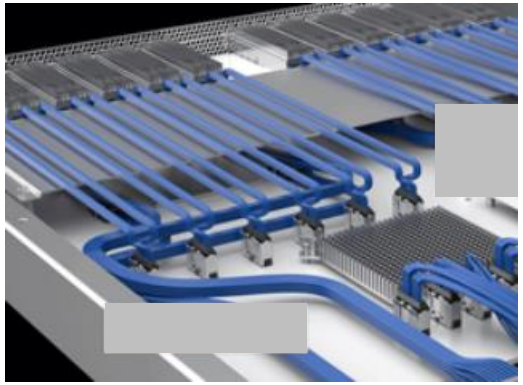
Traditional Line Card and Advanced Technology Alternatives

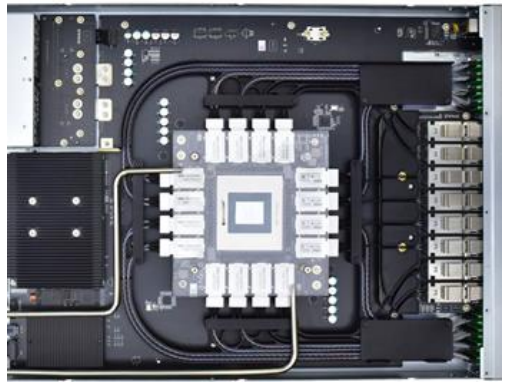
HLC (Horizontal Line Card)

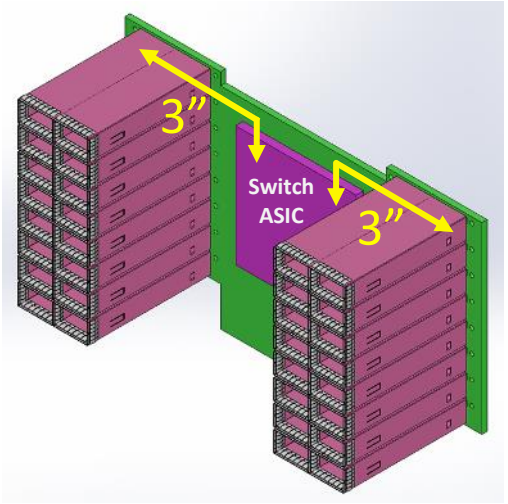
VLC (Vertical Line Card)

Front Pluggable (OSFP, QSFP) Stripline in PCB	Front Pluggable (OSFP, QSFP) Twinax over PCB	Assembled on PCB Near ASIC Package (NPO)	Front Pluggable (OSFP, QSFP) Stripline in PCB









IEEE P802.3 Electrical I/O Specifications (AUI)

- Historically driven by KR (backplane) and CR (copper cable) applications
- Lower loss applications such as C2M (chip to module) not optimized for
- Single AUI specification and single all-purpose SerDes at each data rate
- To maintain the paradigm, CR reach has decreased with increasing data rate:
  - 10G/lane: 15m
  - 25G/lane: 5m
  - 100G/lane: 2m
  - 200G/lane: 1m (approved objective for current 802.3dj Task Force)
- 802.3dj TF realized that a single ~36dB loss SerDes is suboptimum for lower loss applications

IEEE P802.3dj AUI Objectives

- With strong support, IEEE 802.3dj adopted two 200 Gbps/lane AUI C2M objectives:
  A. Medium loss (~22 dB IL)
  B. High loss (~36 dB IL)
- Advanced Technologies that are optimally supported by medium loss (~22 dB) spec:
  - Strip-line to center front panel slots (<5”) on conventional line cards
  - Twinax over PCB
  - NPO
  - VLC

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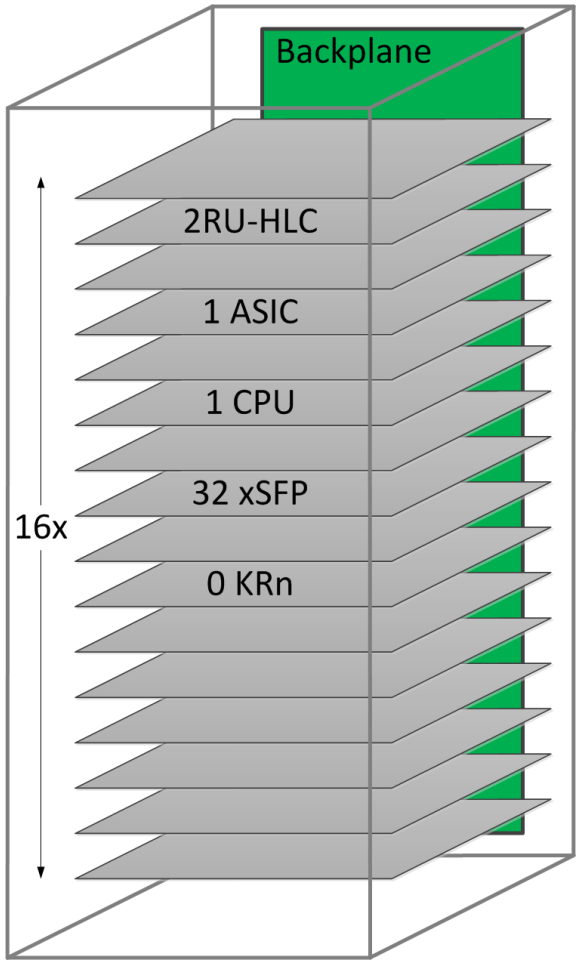
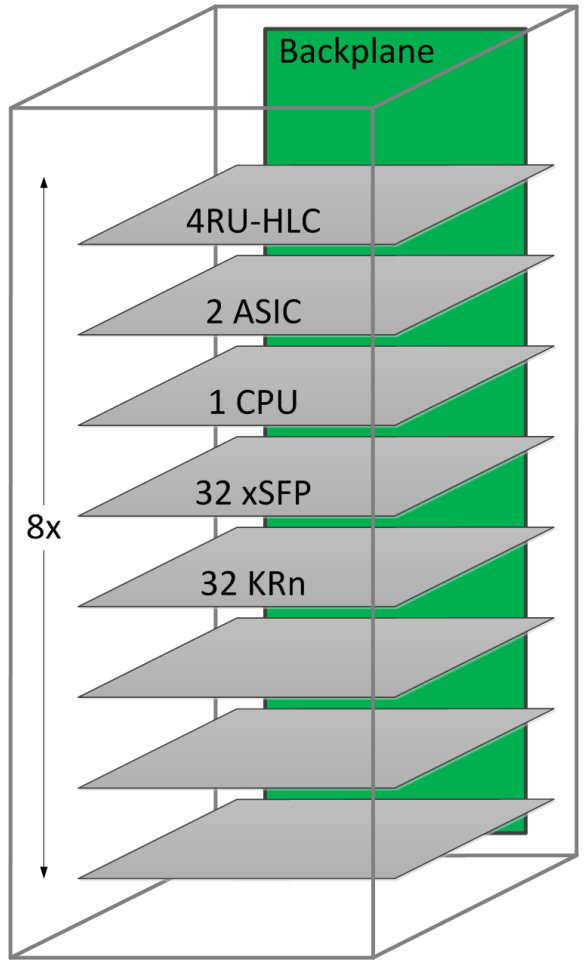
2RU-HLC 16x

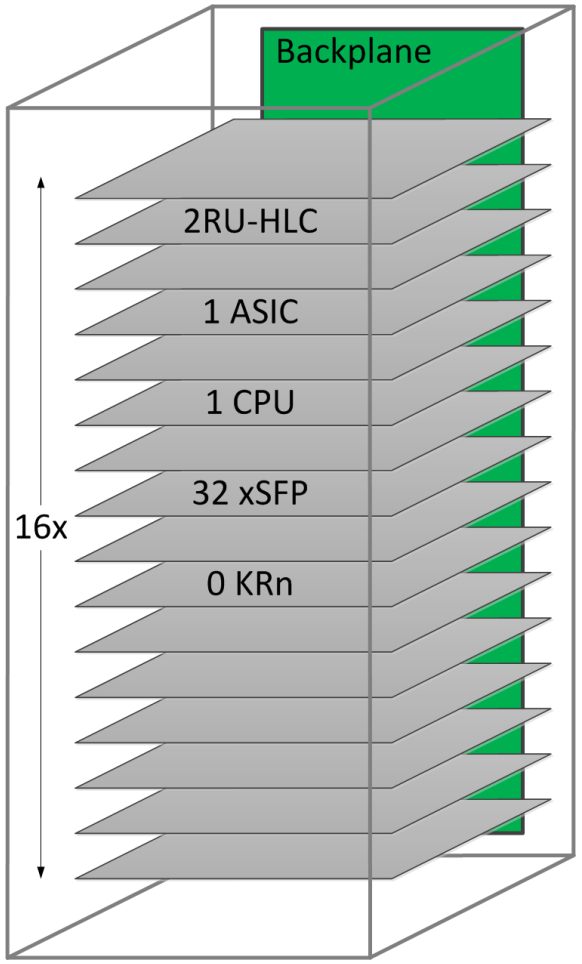


4RU-HLC 8x

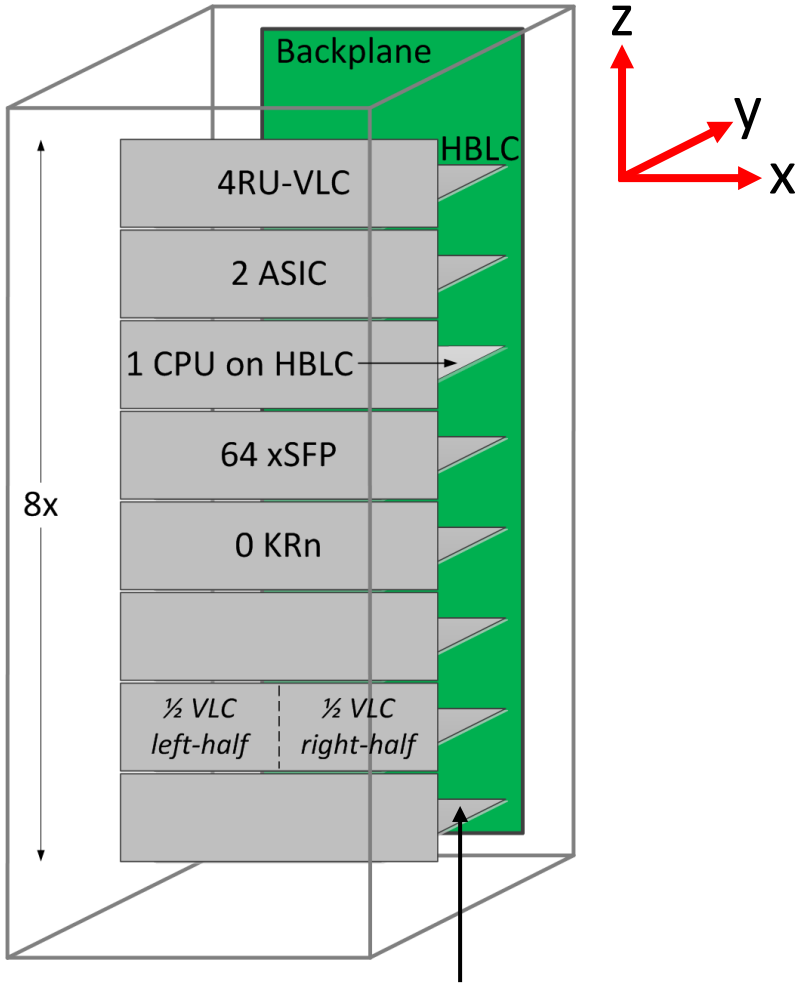


Fabric application

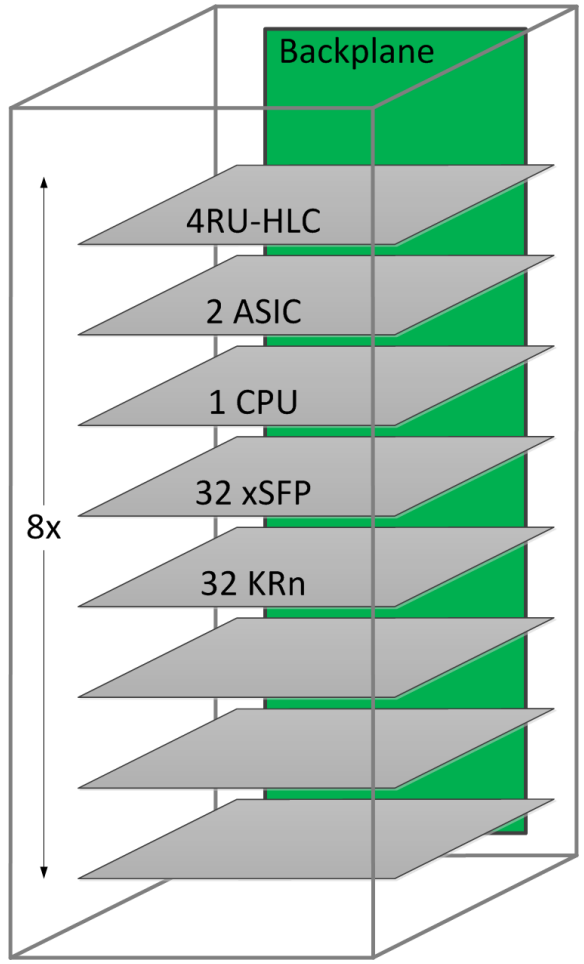
2RU-HLC 16x



4RU-VLC 8x



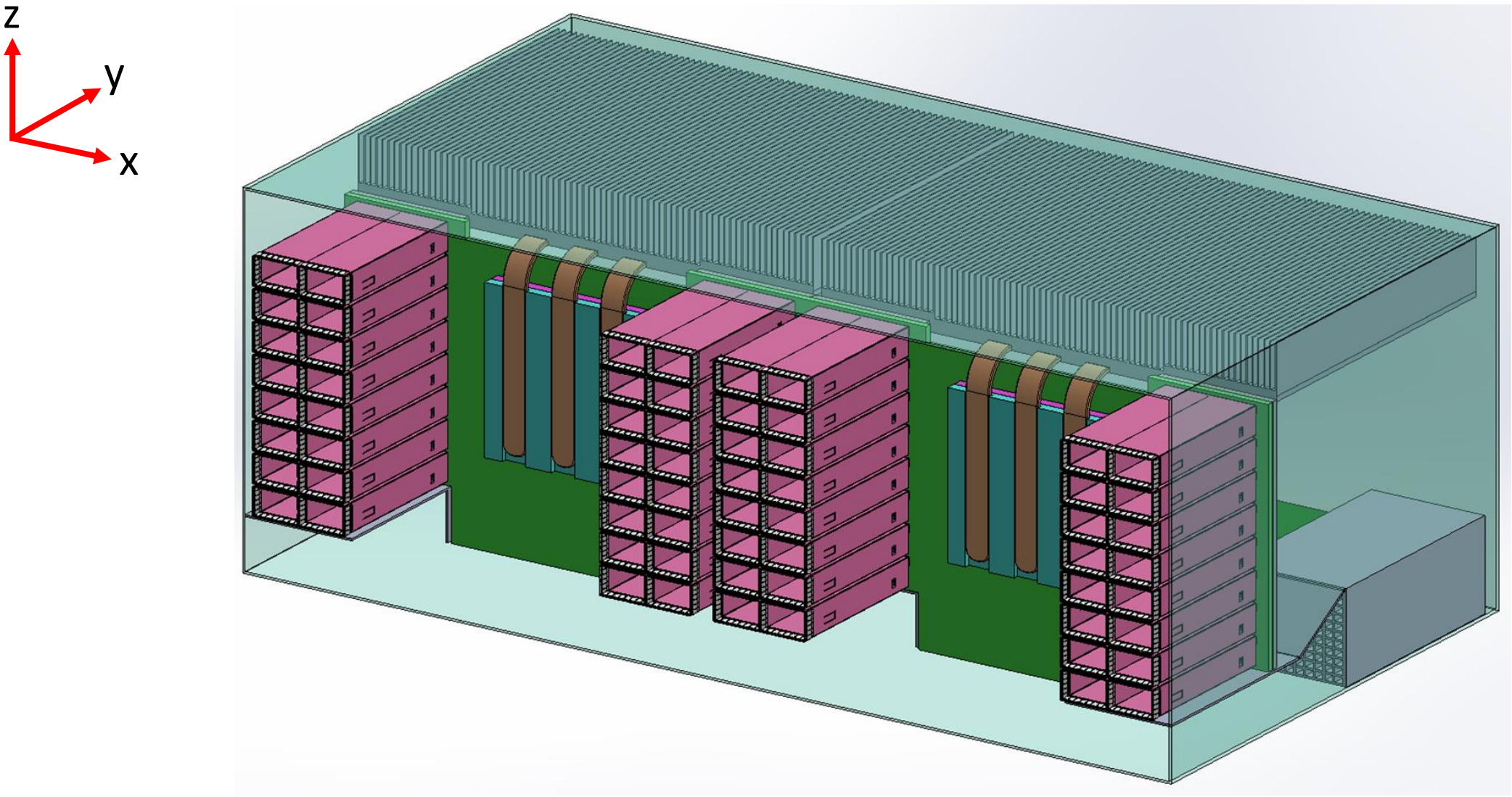
4RU-HLC 8x



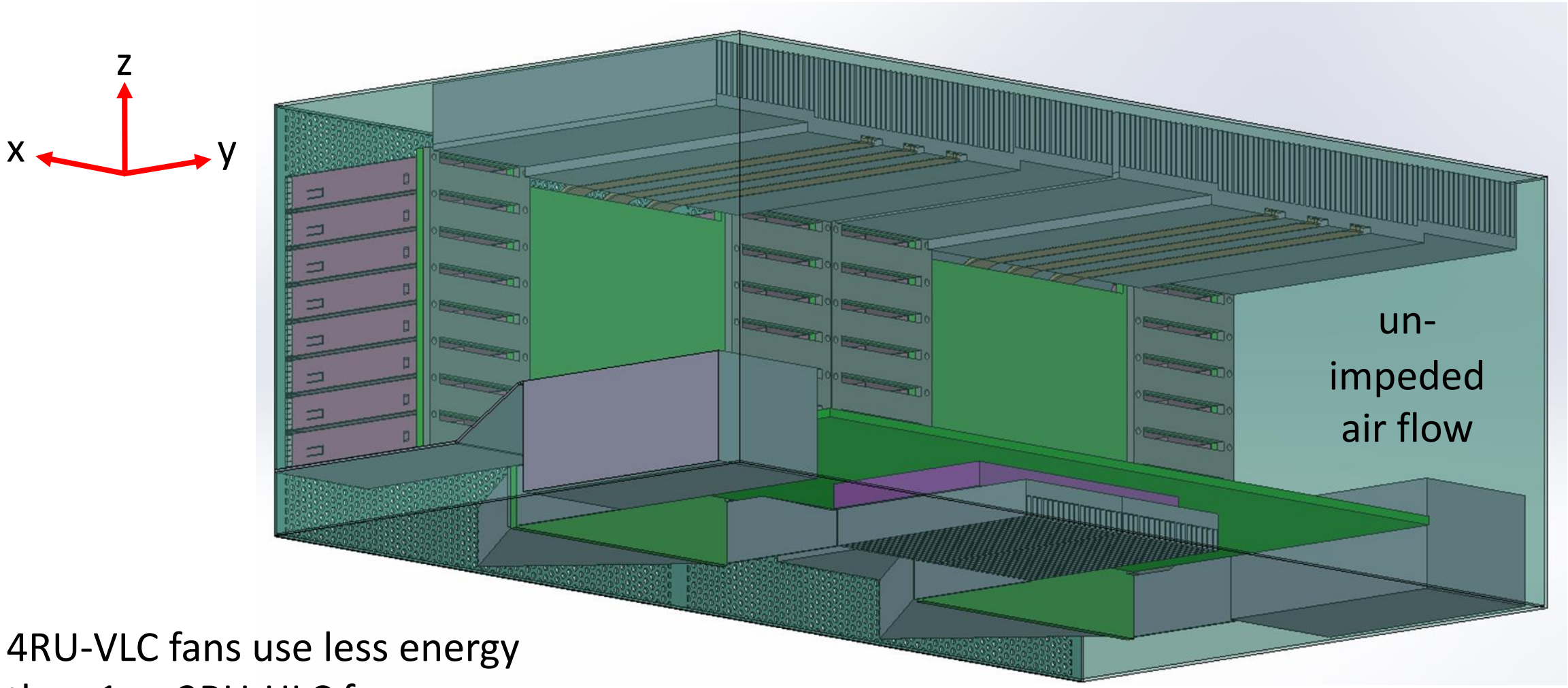
HBLC := Horizontal Back Line Card

Fabric application

4RU-VLC, 64 OSFP, 2 Front ASIC (Assembly Front 3-D View)

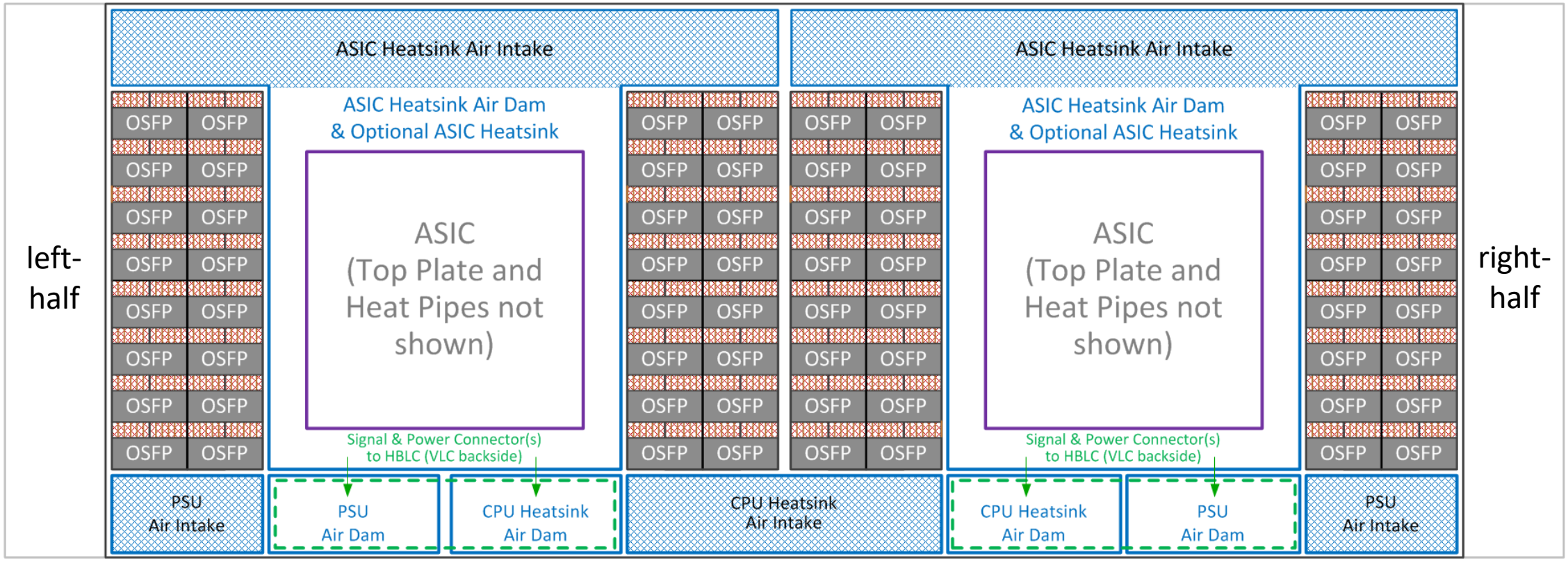


4RU-VLC, 64 OSFP, 2 Front ASIC (Assembly Rear 3-D View)

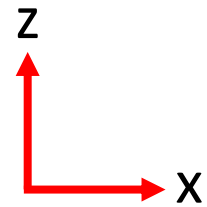


4RU-VLC fans use less energy
than 1 or 2RU-HLC fans

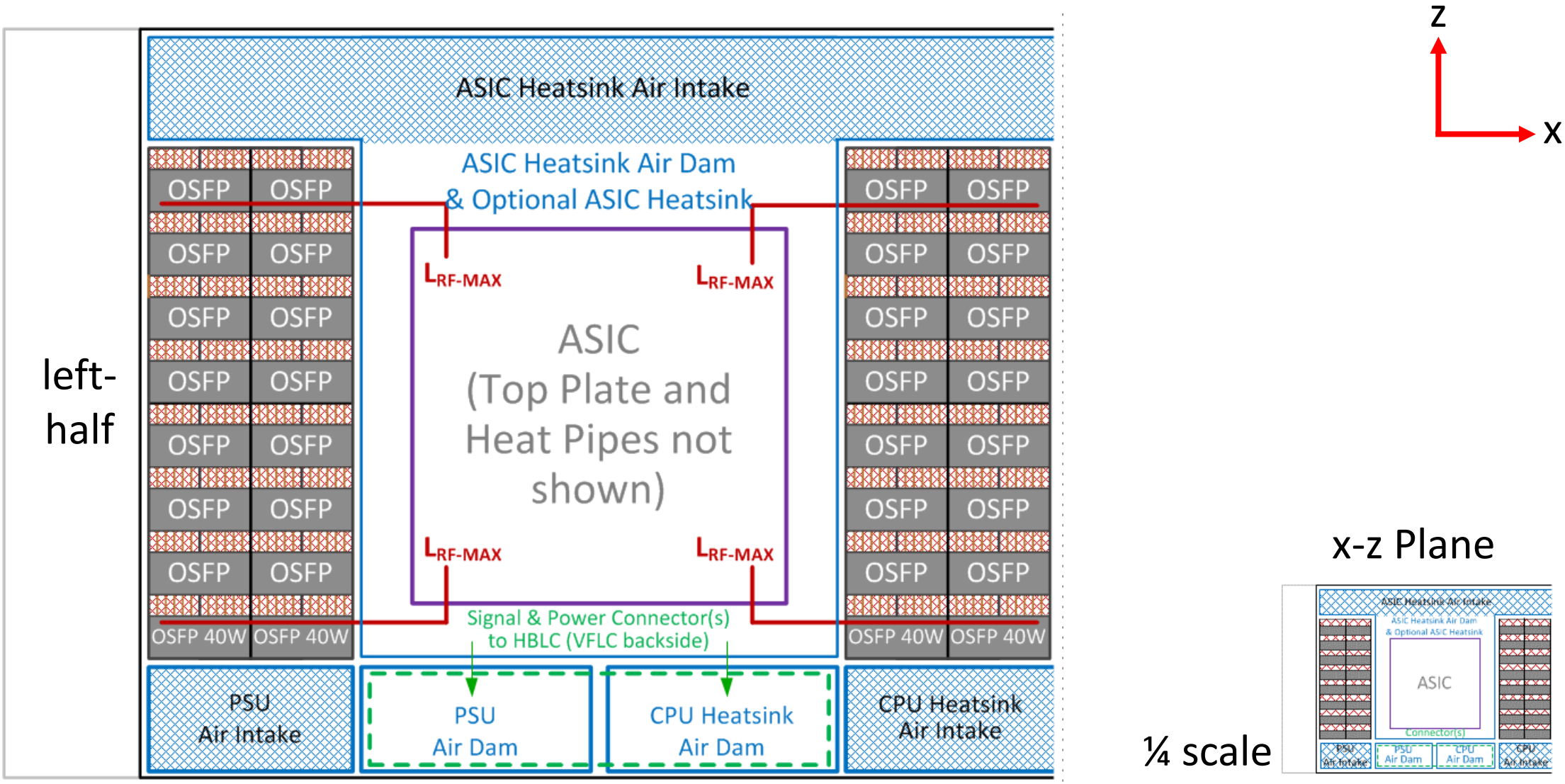
4RU-VLC, 64 OSFP, 2 Front ASIC, 3.3” $L_{RF\text{-}MAX}$ (Full Front View)



- OSFP vertical pitch = 15mm (MSA spec)
  horizontal pitch = 24mm
- PCB Stripline $L_{RF\text{-}MAX}$ =
  72mm + 12mm = 84mm **(3.3")**



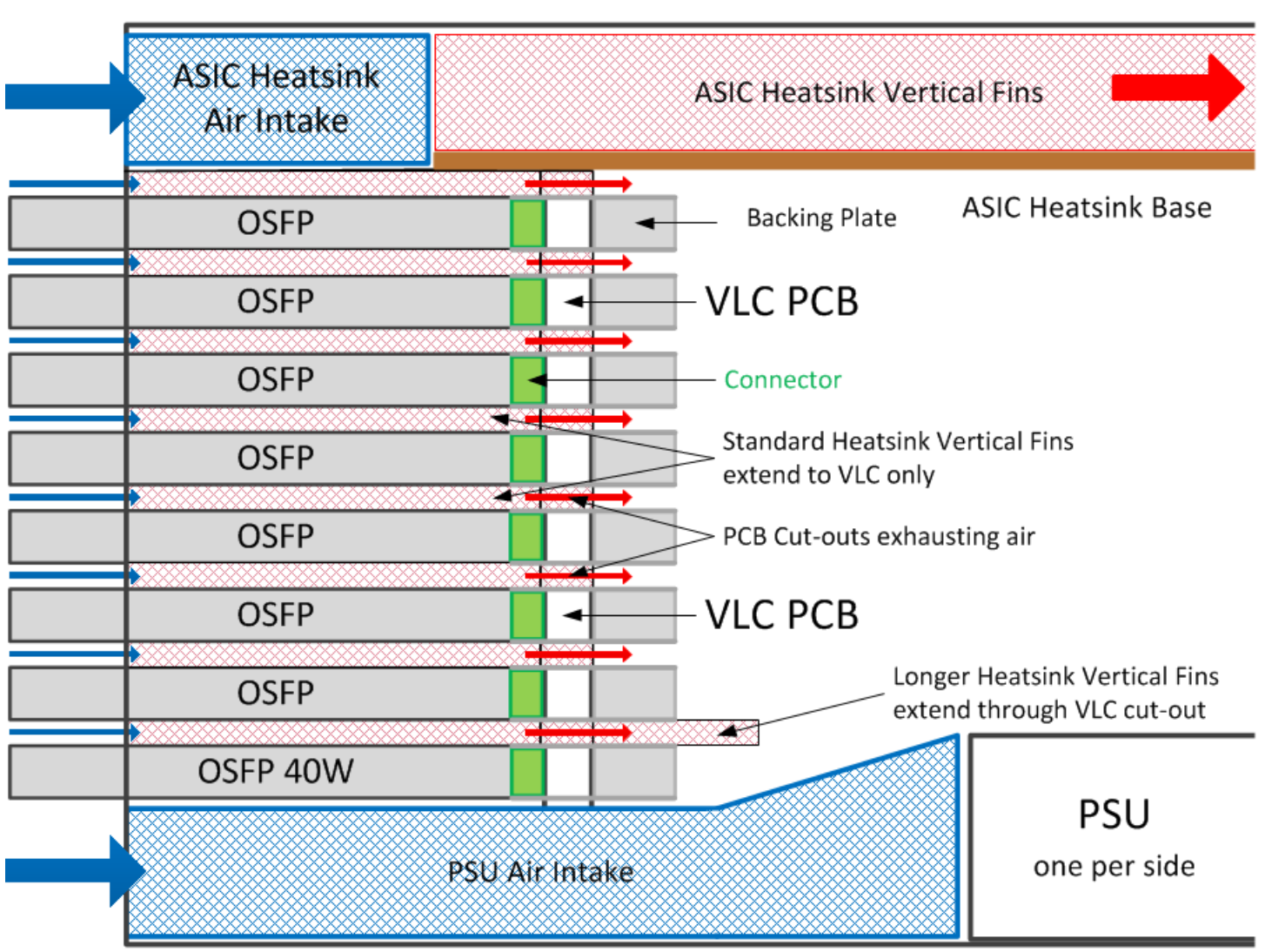
4RU-VLC, 64 OSFP, 2 Front ASIC, 3.3” $L_{RF\text{-}MAX}$ (Left-half Front View)



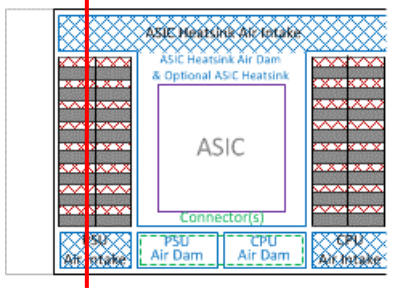
x-z Plane

¼ scale

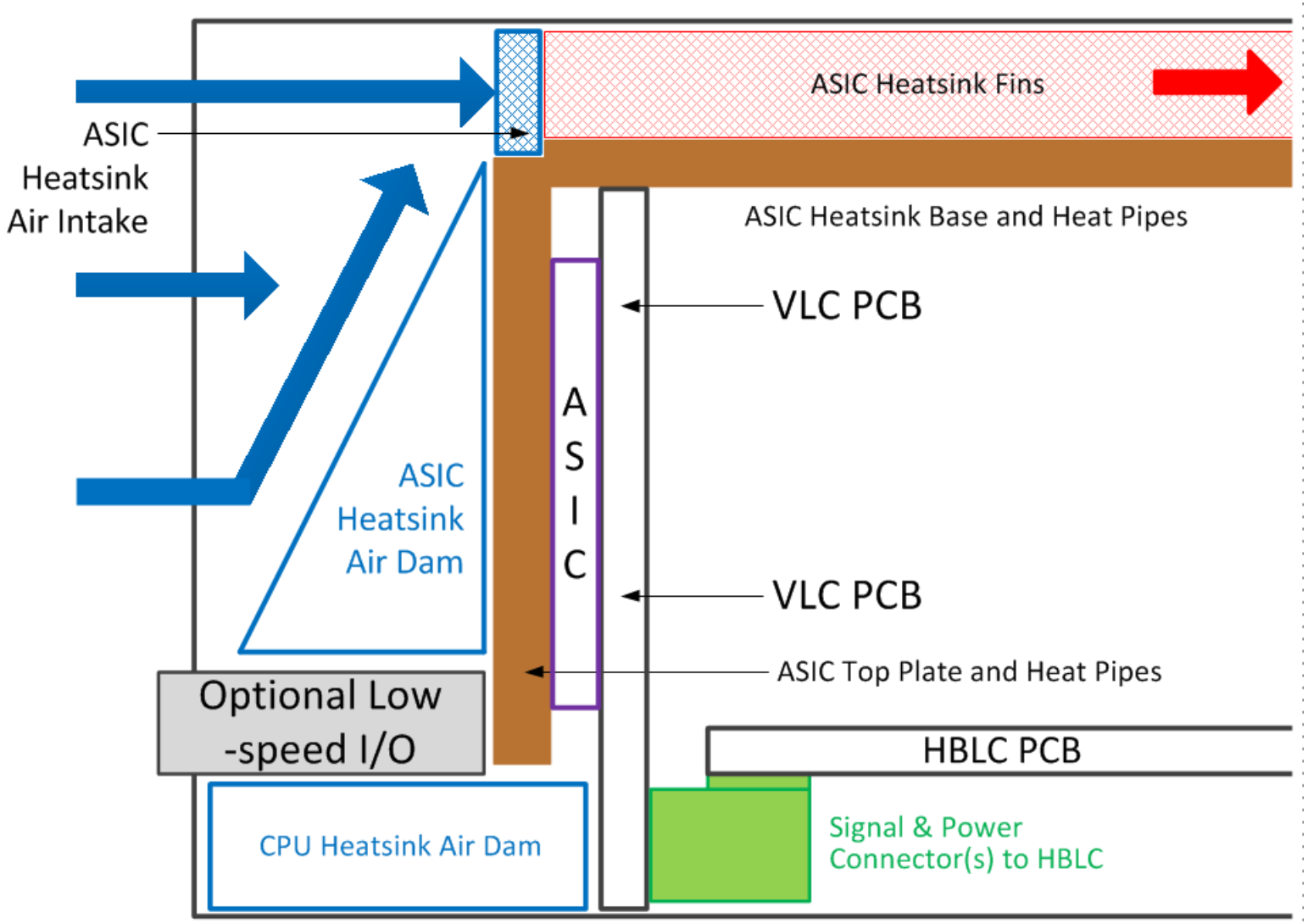
4RU-VLC, 64 OSFP, 2 Front ASIC (y-z Plane 1 Front-half Side View)

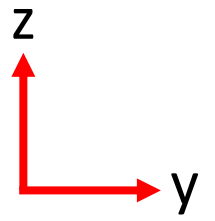


y-z
Plane 1

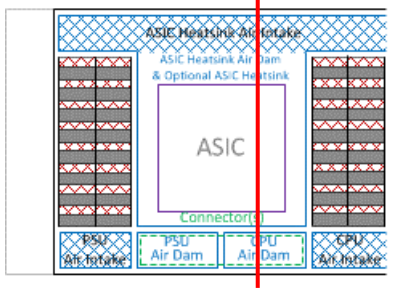


4RU-VLC, 64 OSFP, 2 Front ASIC (y-z Plane 2 Front-half Side View)

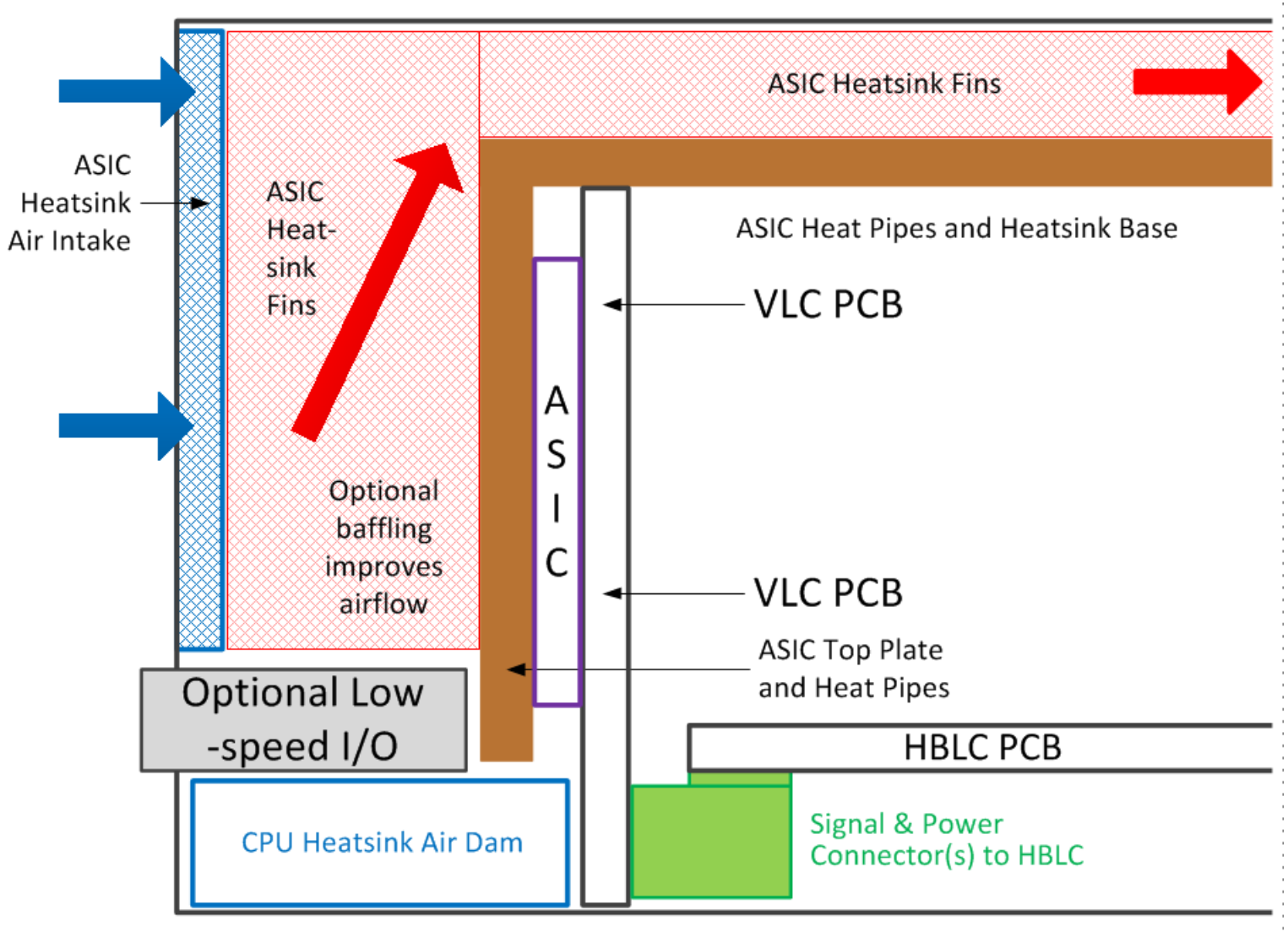


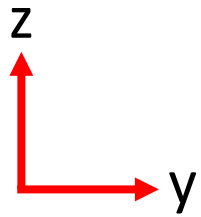


y-z Plane 2

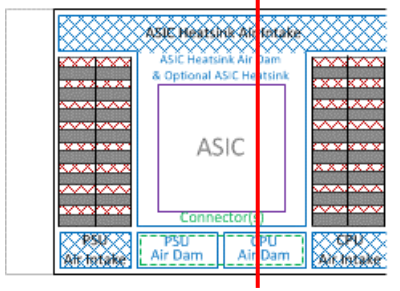


4RU-VLC, 64 OSFP, 2 Front ASIC (y-z Plane 2 Front-half Side View)

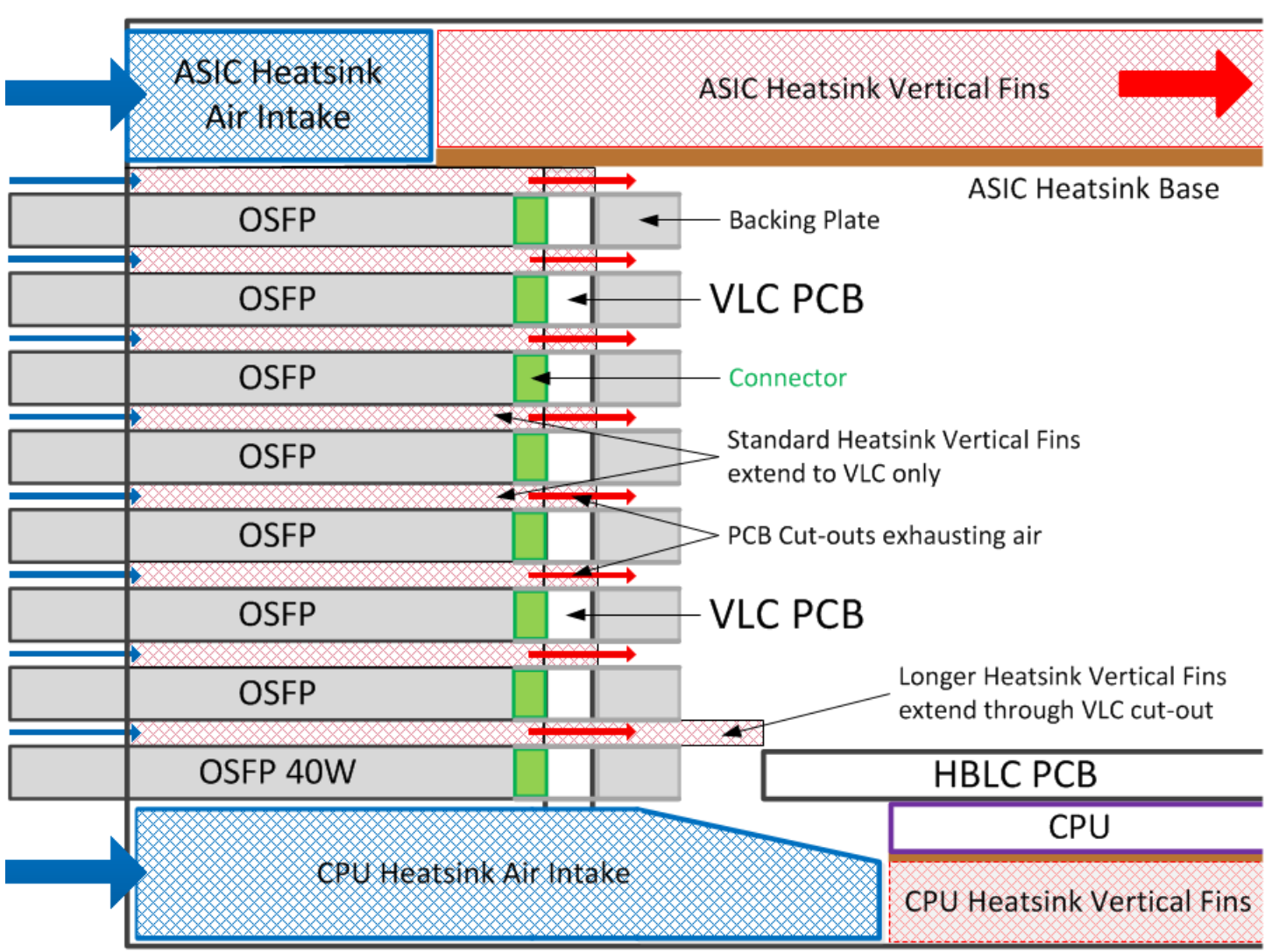


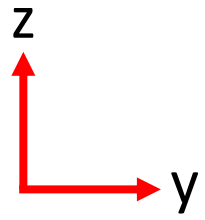


y-z
Plane 2

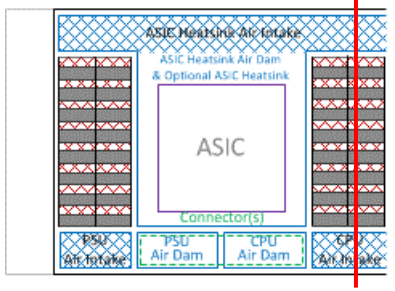


4RU-VLC, 64 OSFP, 2 Front ASIC (y-z Plane 3 Front-half Side View)

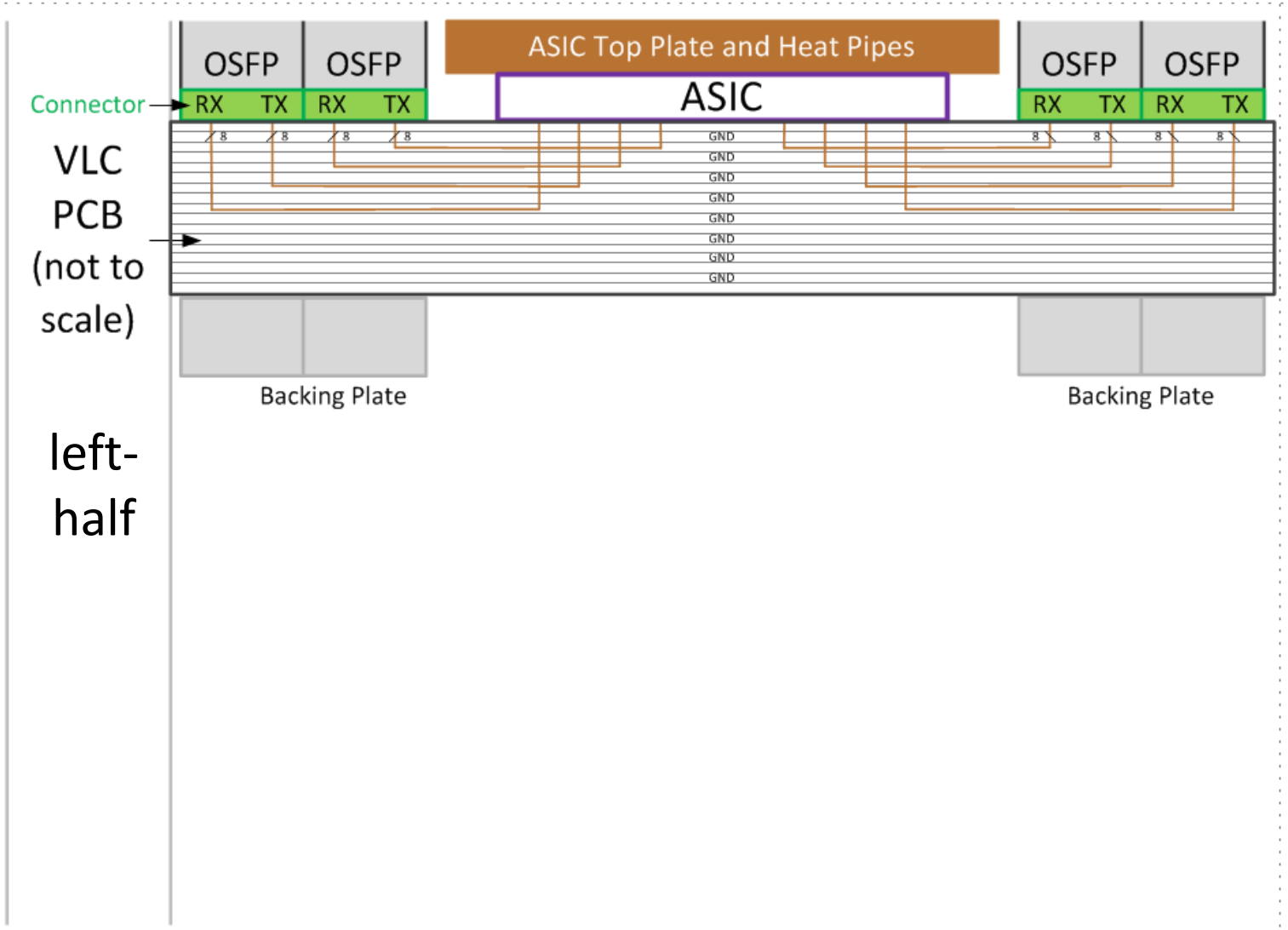


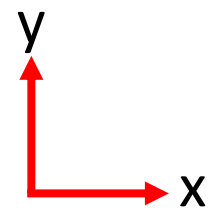


y-z
Plane 3

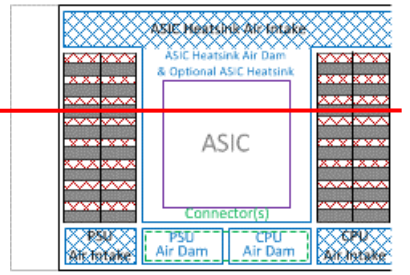


4RU-VLC, 64 OSFP, 2 Front ASIC (x-y Plane 4 Left-half Top View)

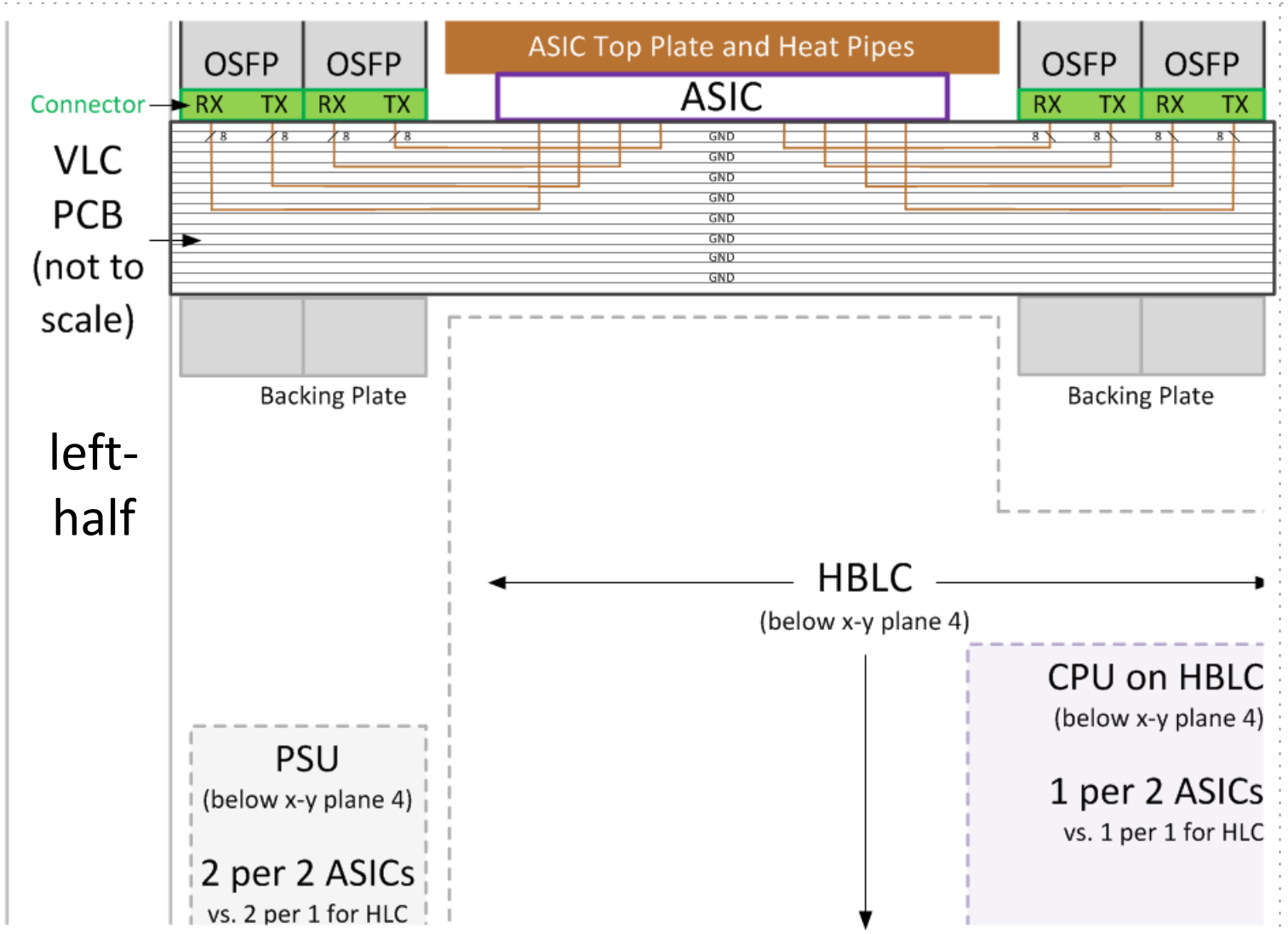


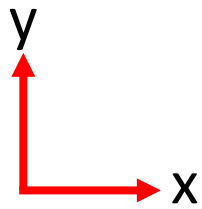


x-y
Plane 4

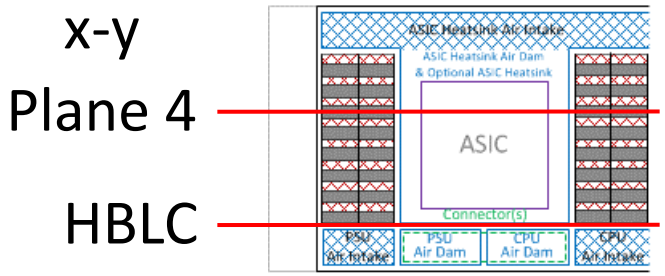


4RU-VLC, 64 OSFP, 2 Front ASIC (x-y Plane 4 Left-half Top View)

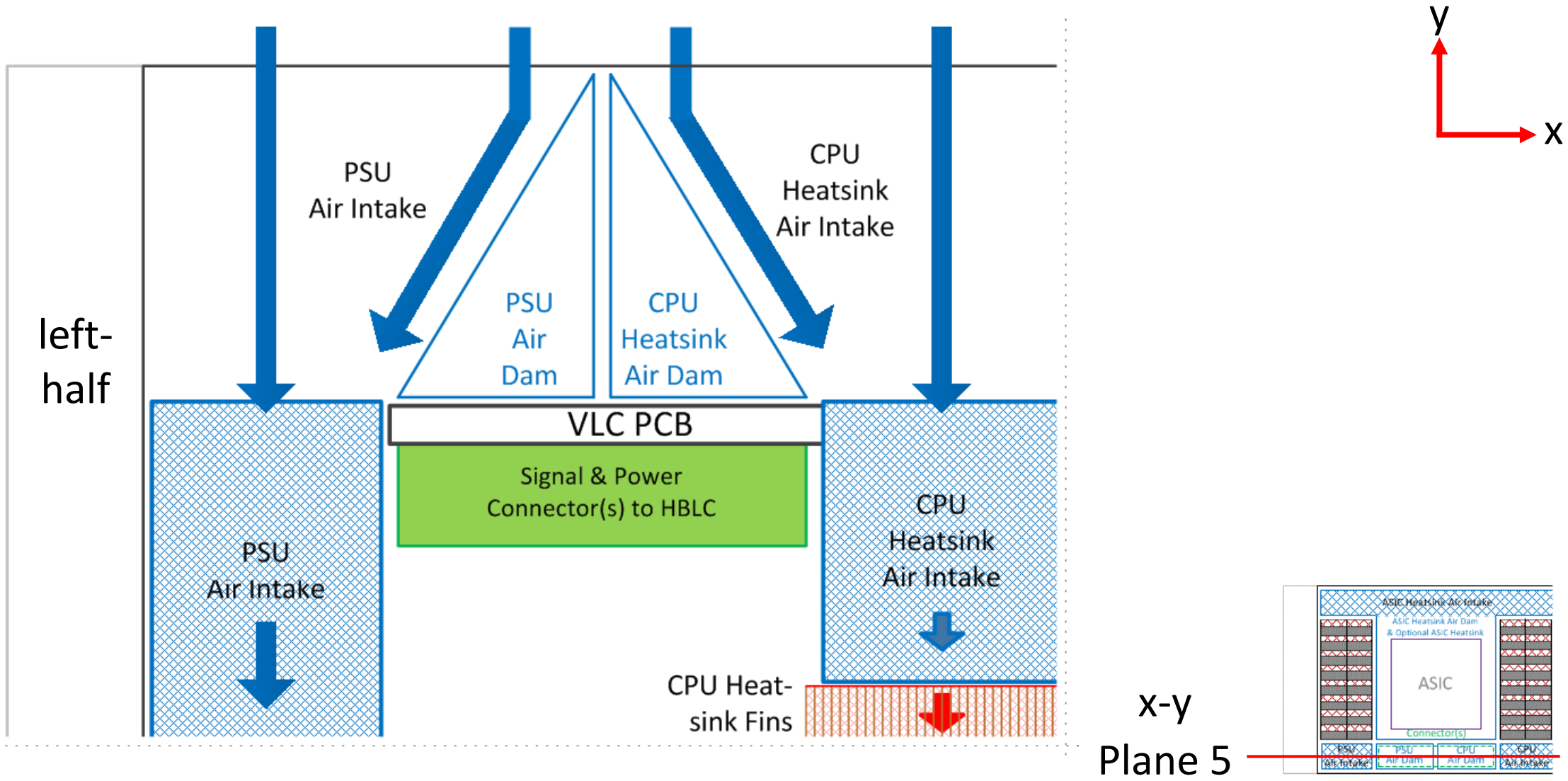




ASIC and CPU on separate PCBAs decouples design and chip generations



4RU-VLC, 64 OSFP, 2 Front ASIC (x-y Plane 5 Left-half Top View)



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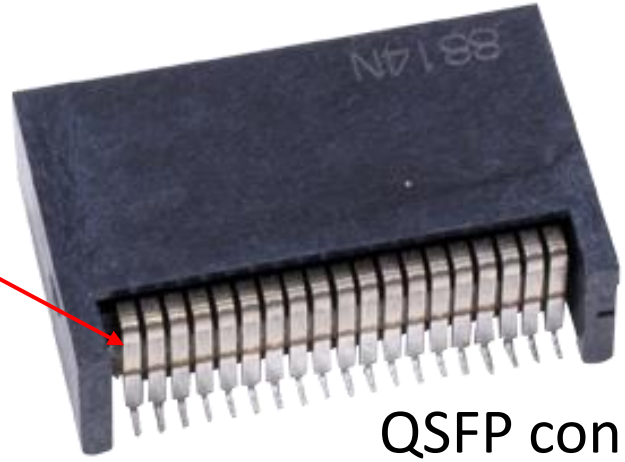
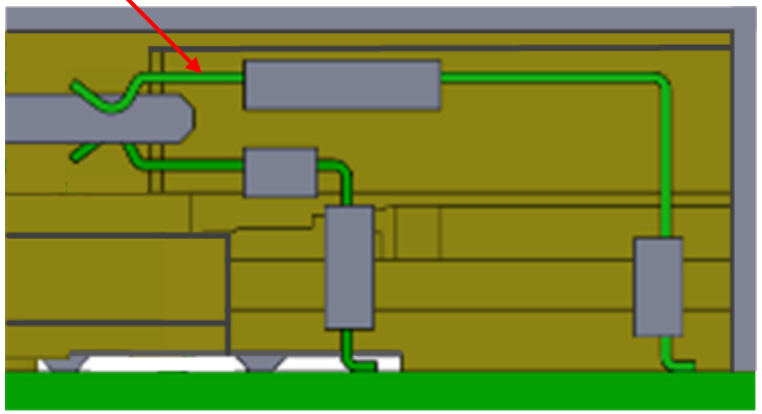
Horizontal Line Card Connector

top row lead



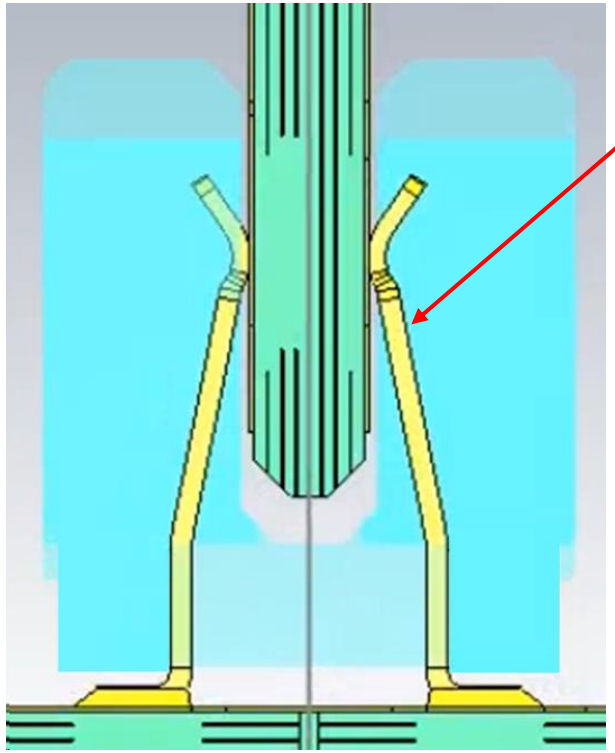
QSFP connector



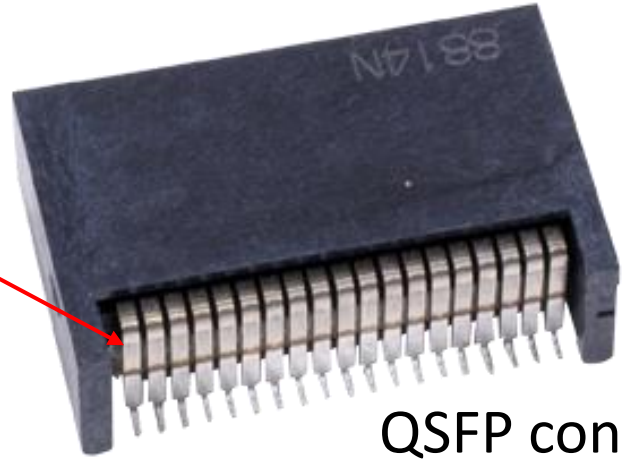
HLC

Vertical vs. Horizontal Line Card Connector

top row lead



VLC



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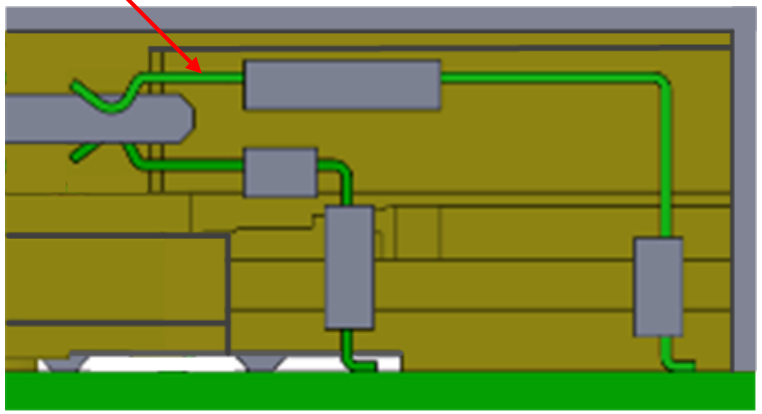
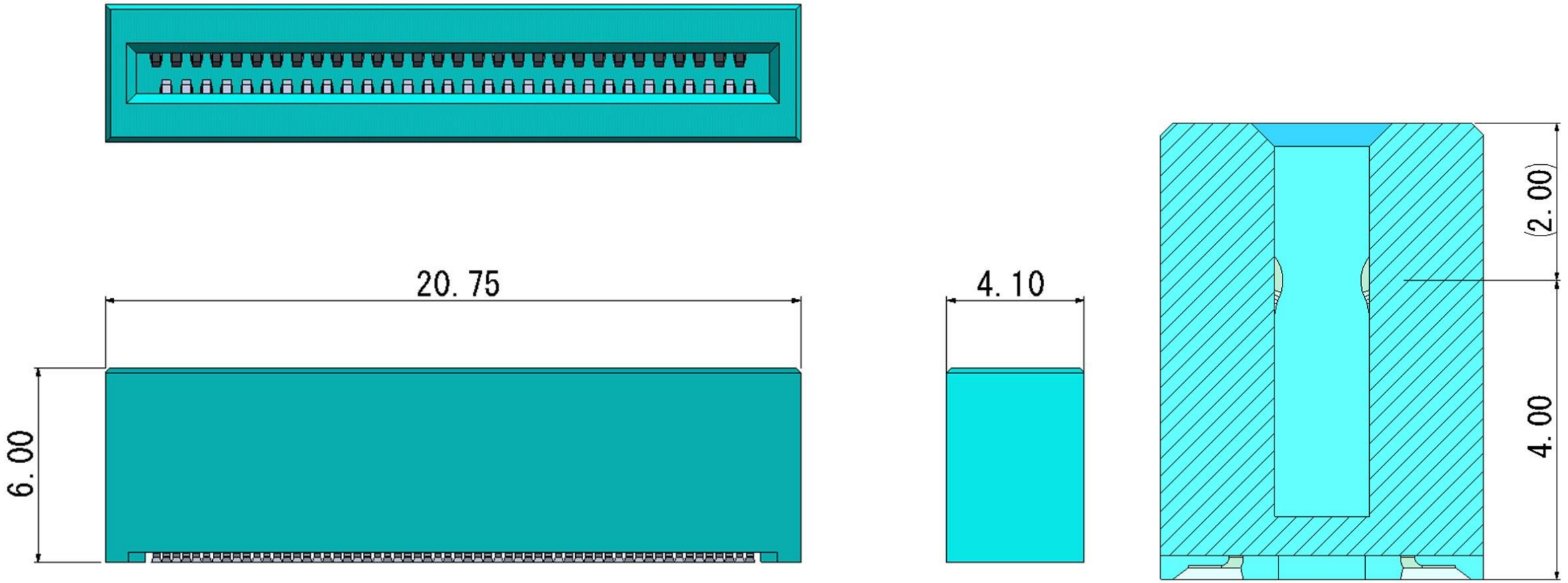
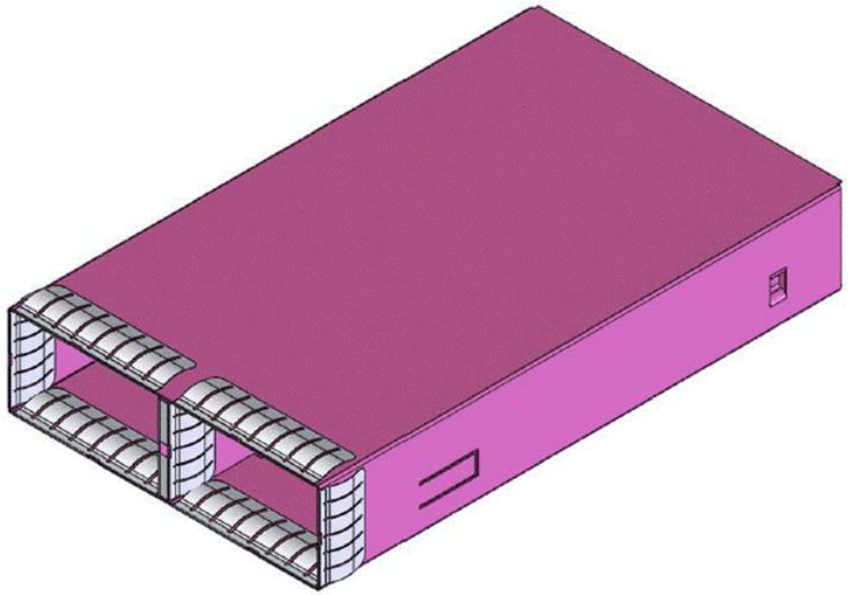


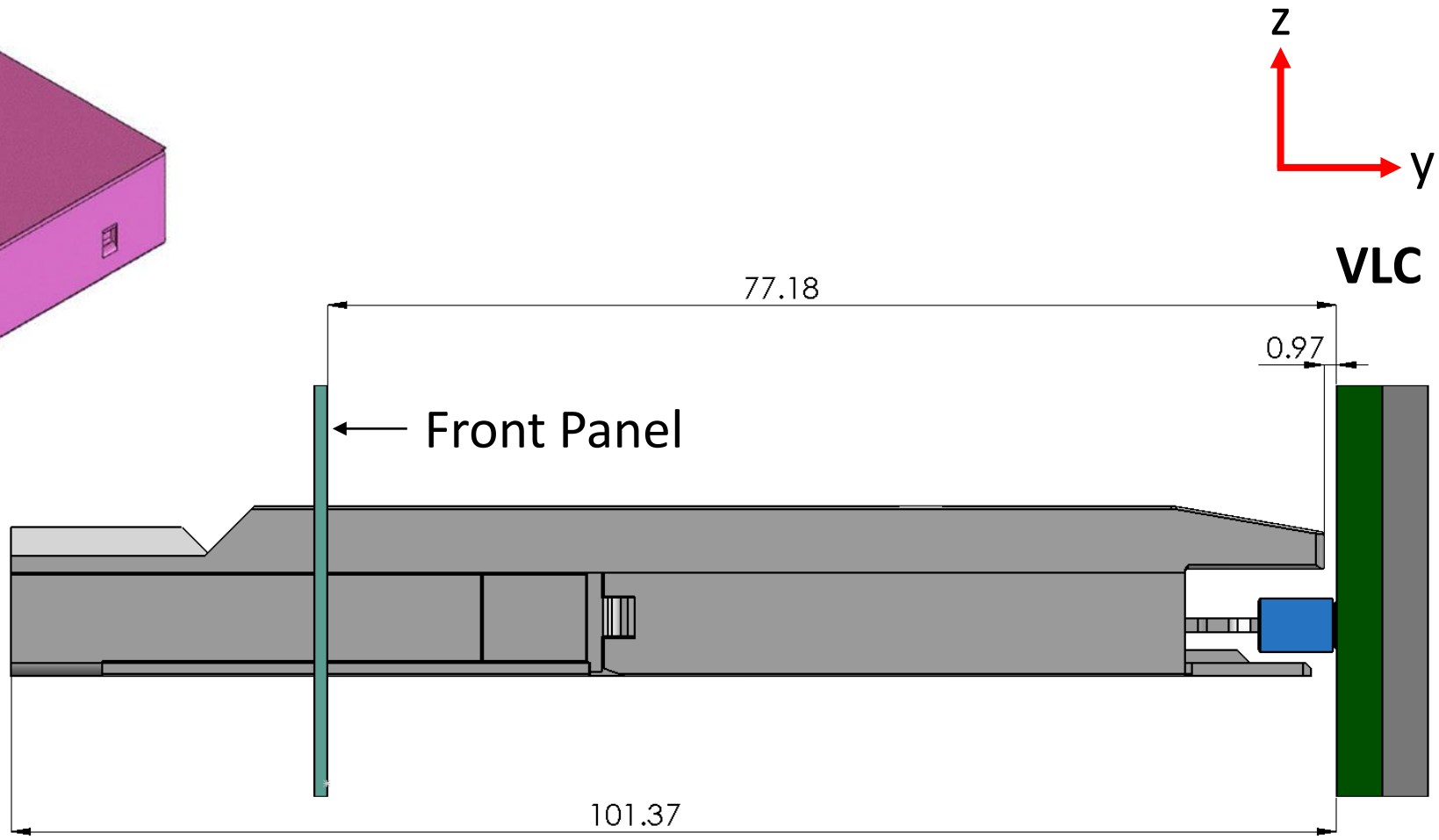
HLC

Vertical OSFP Connector

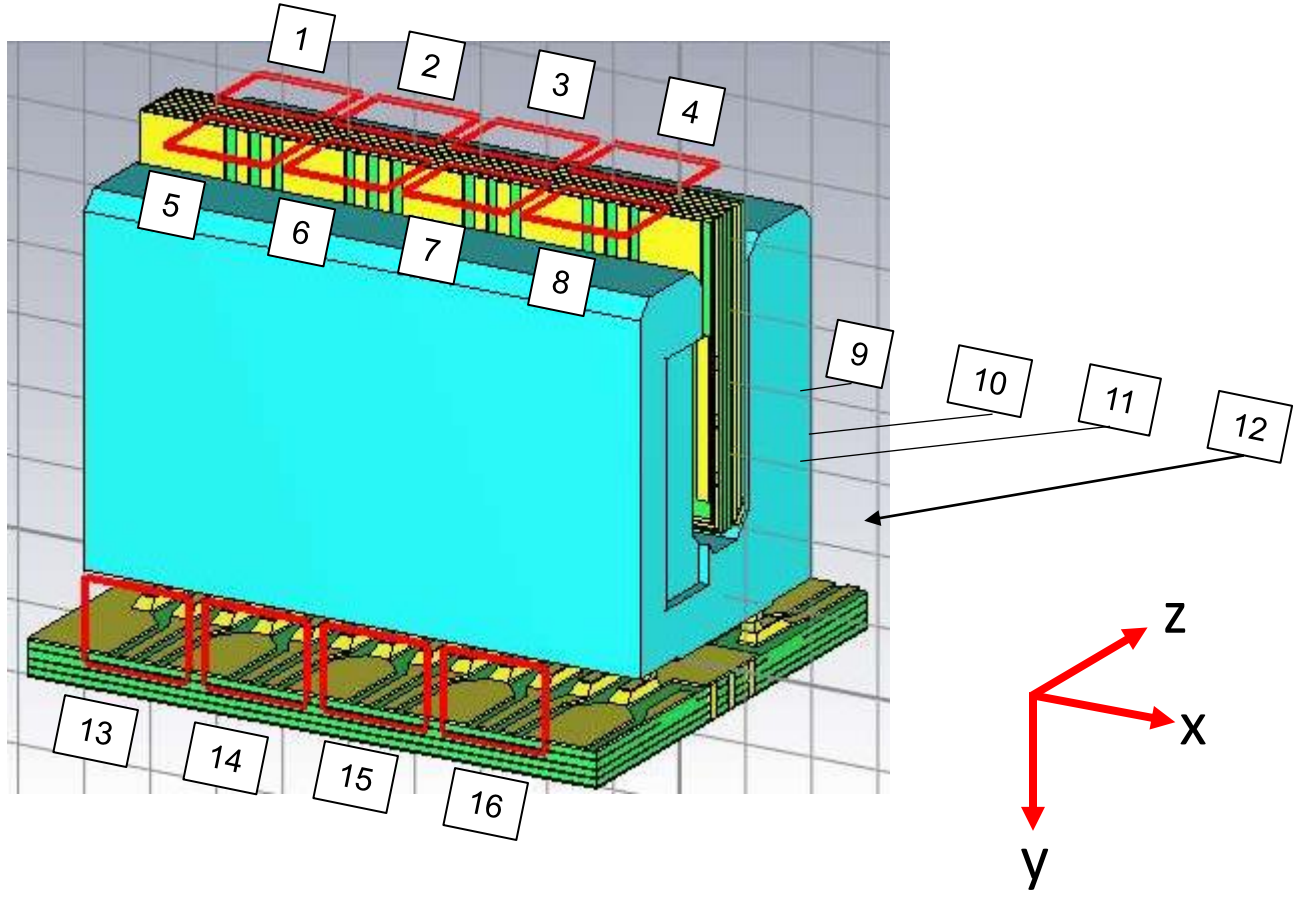


Vertical OSFP Connector Cage & Mating View



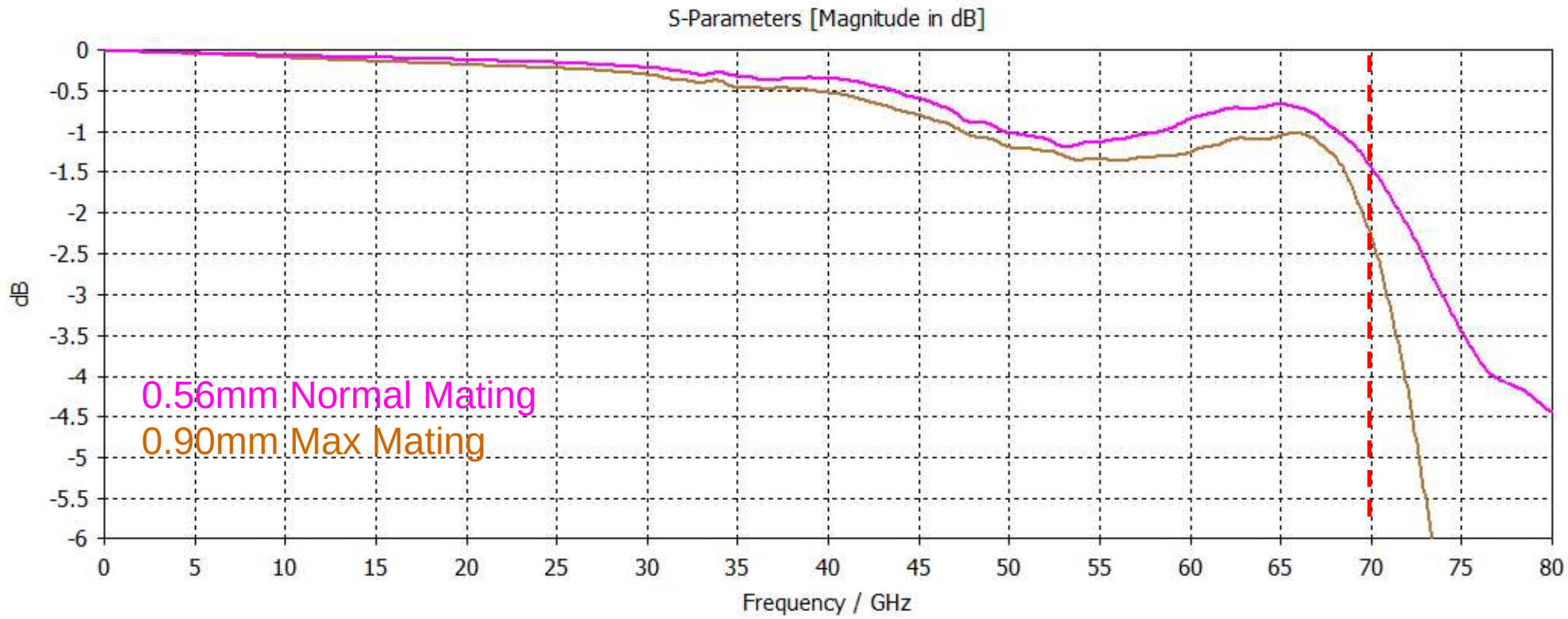


Vertical OSFP Connector Simulation Model



Vertical OSFP Connector Insertion Loss

FEXT & NEXT in Appendix 2



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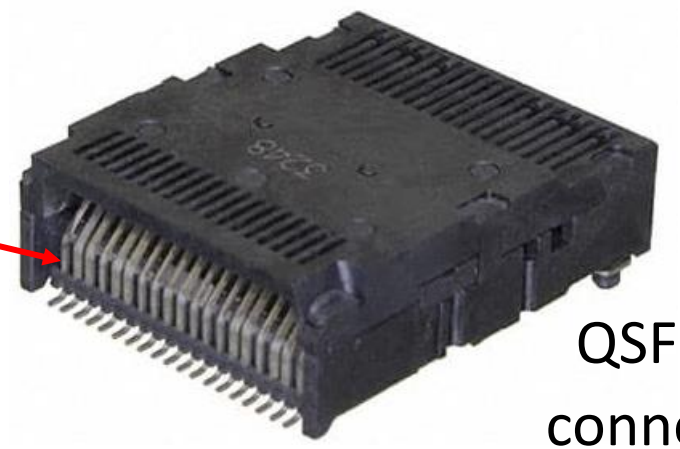
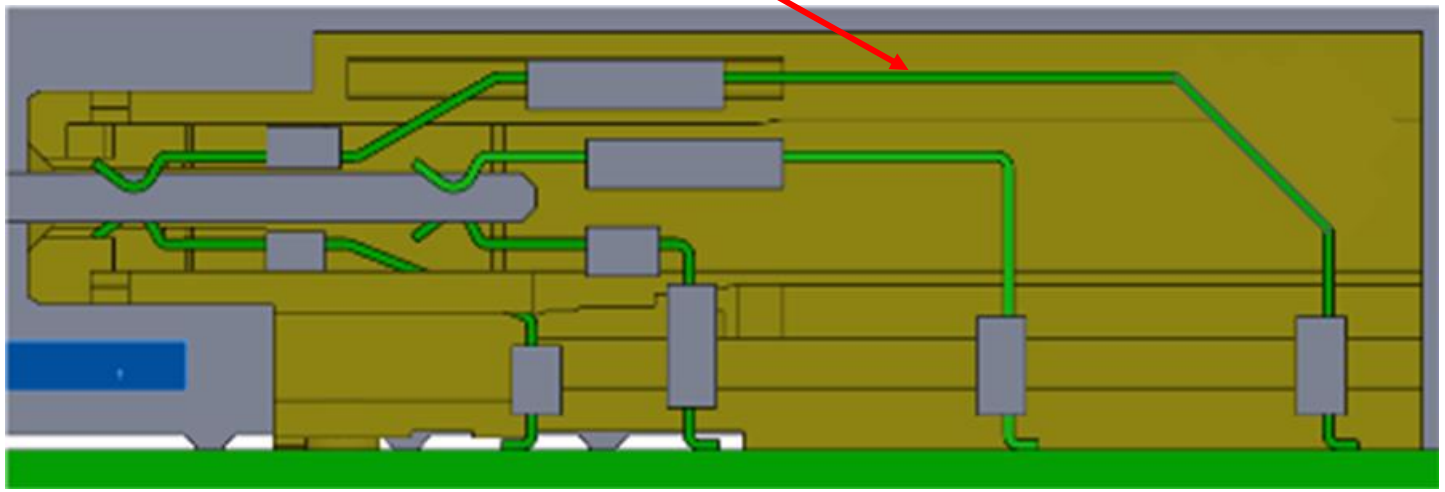
Horizontal Line Card Double Density Connector

top row lead

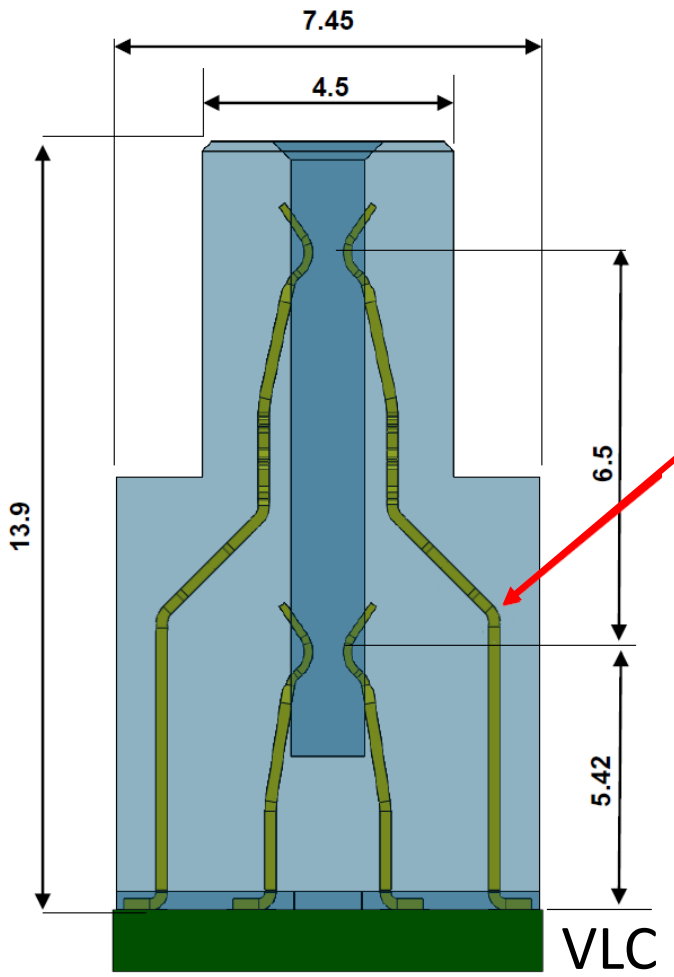


QSFP-DD connector



HLC

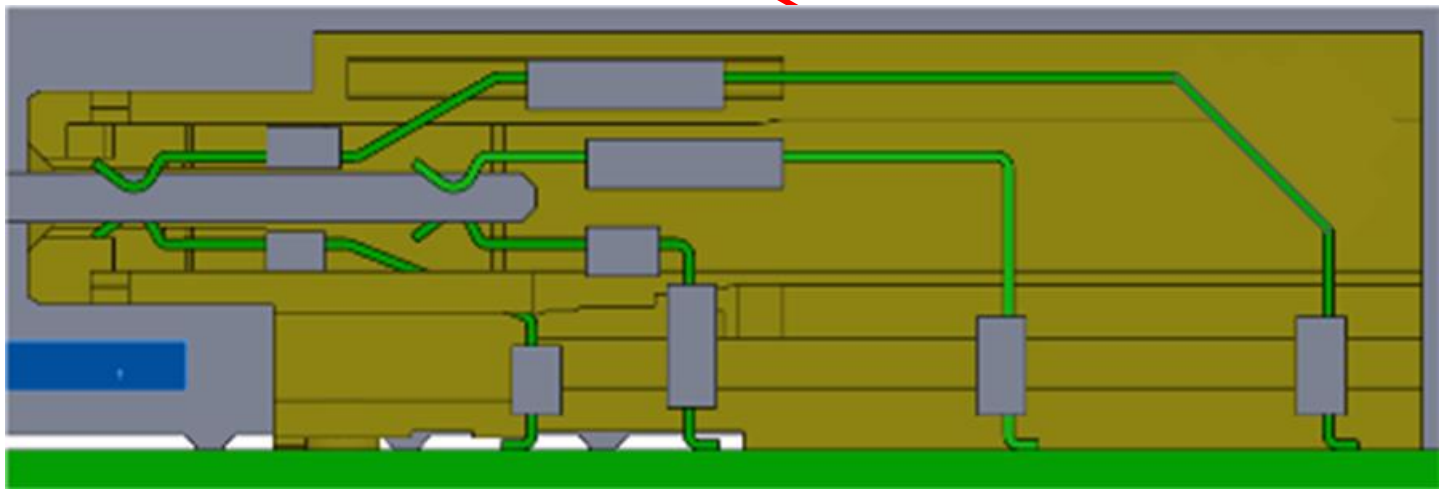
Vertical vs. Horizontal Line Card Double Density Connector



VLC

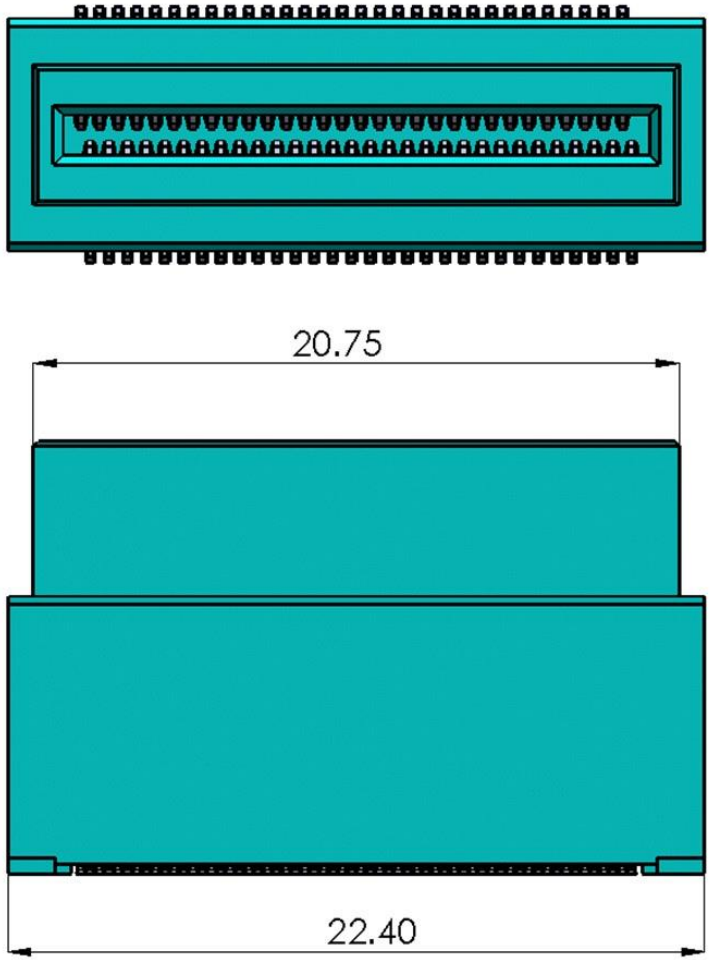
top row lead

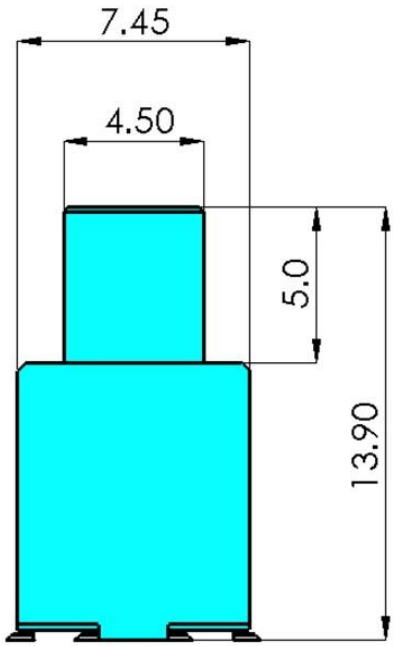
QSFP-DD connector

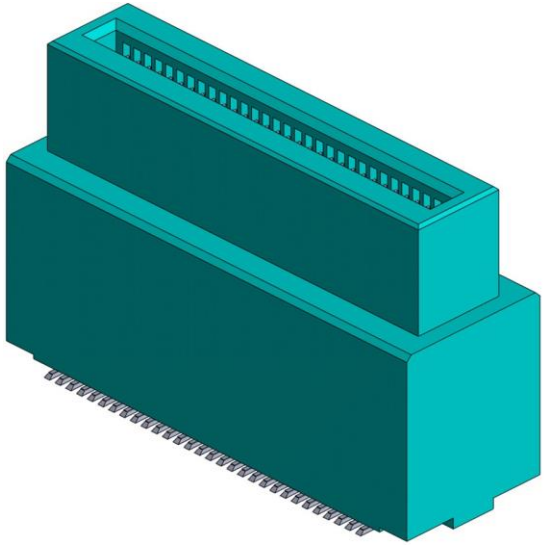


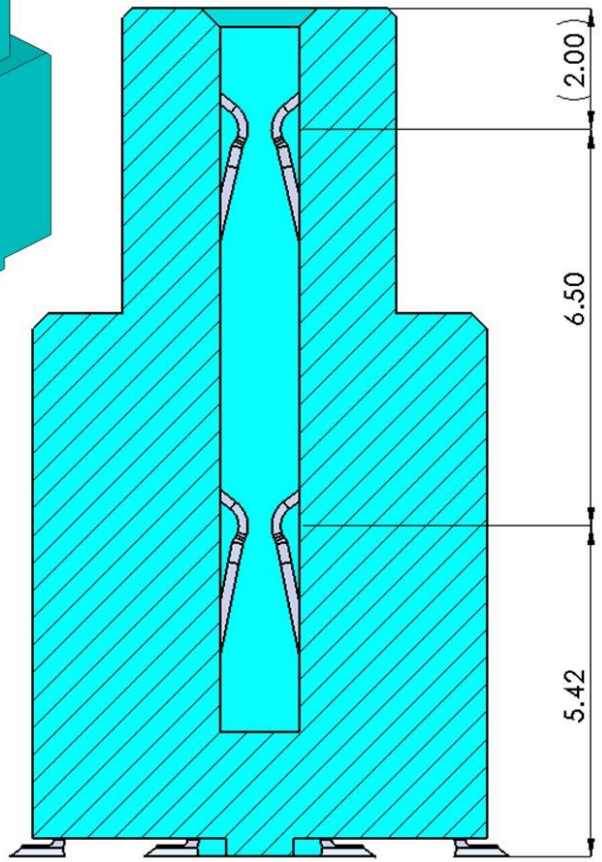
HLC

Vertical OSFP-XD Connector

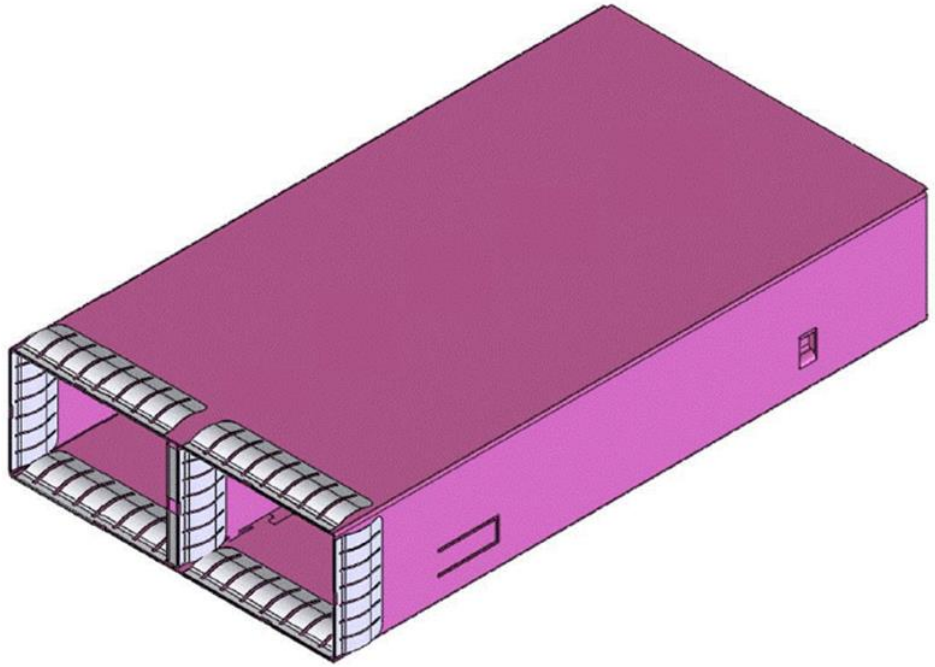


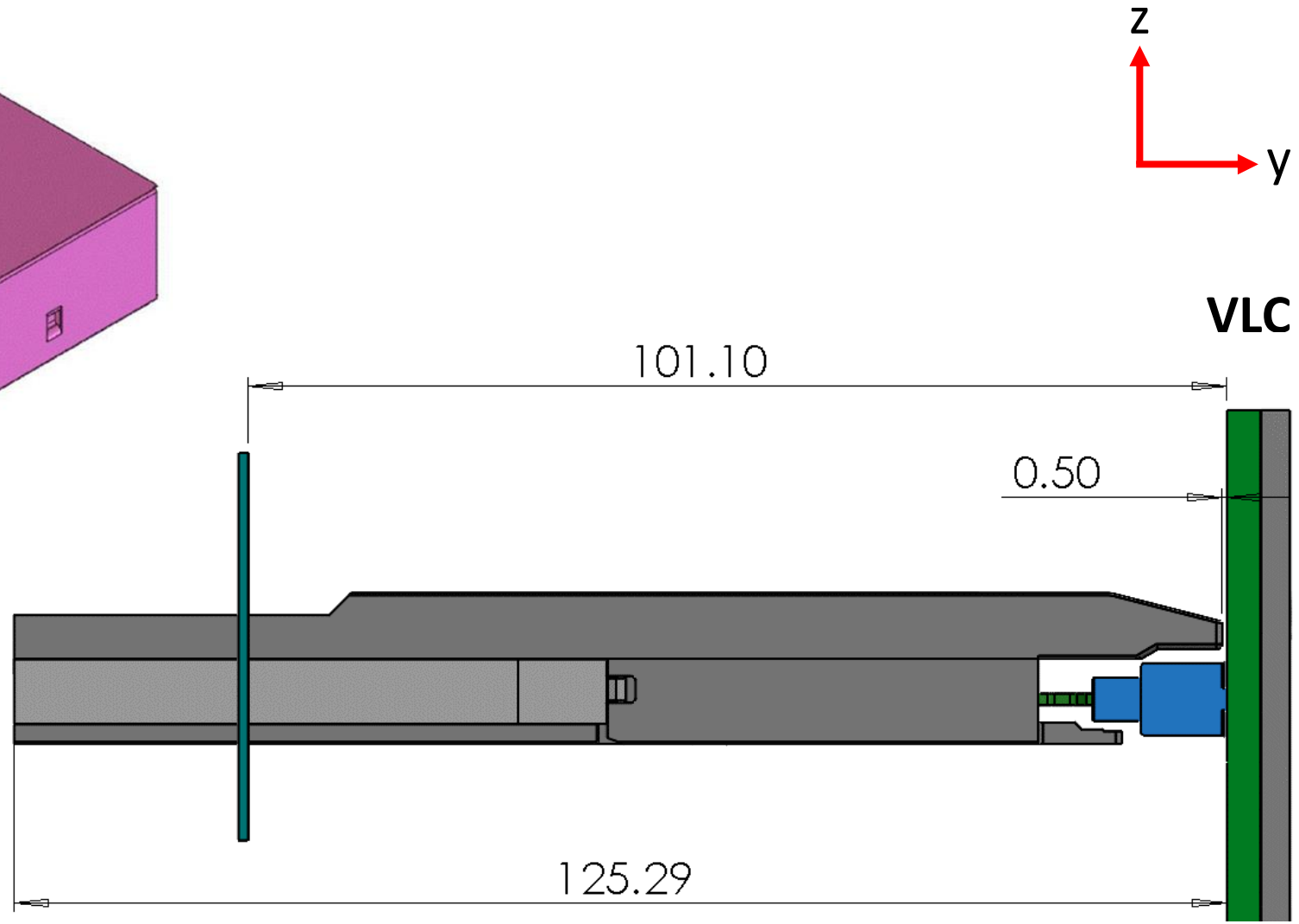




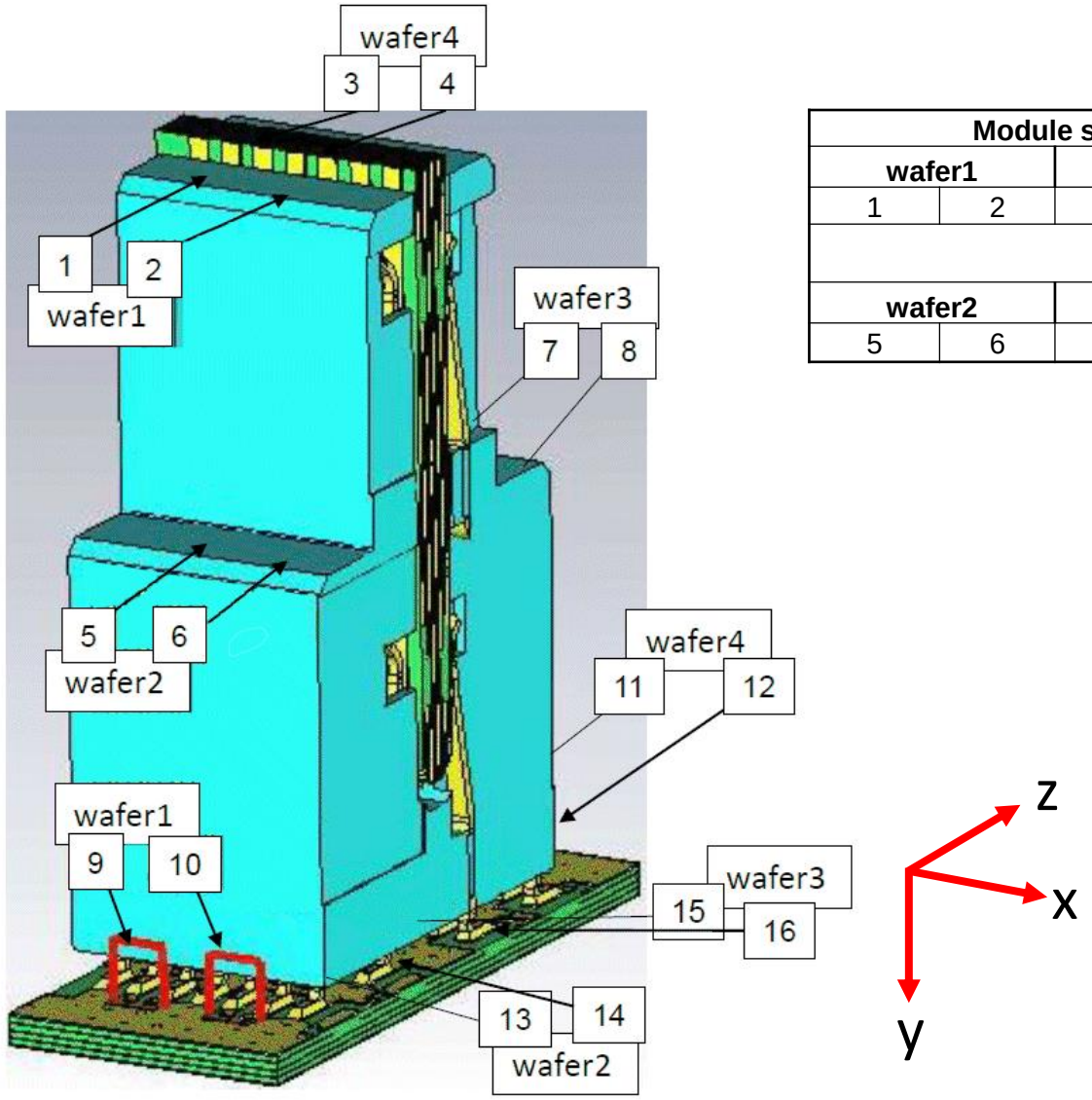


Vertical OSFP-XD Cage & Mating View





Vertical OSFP-XD Connector Simulation Model



Module side			
wafer1		wafer4	
1	2	3	4
wafer2		wafer3	
5	6	7	8

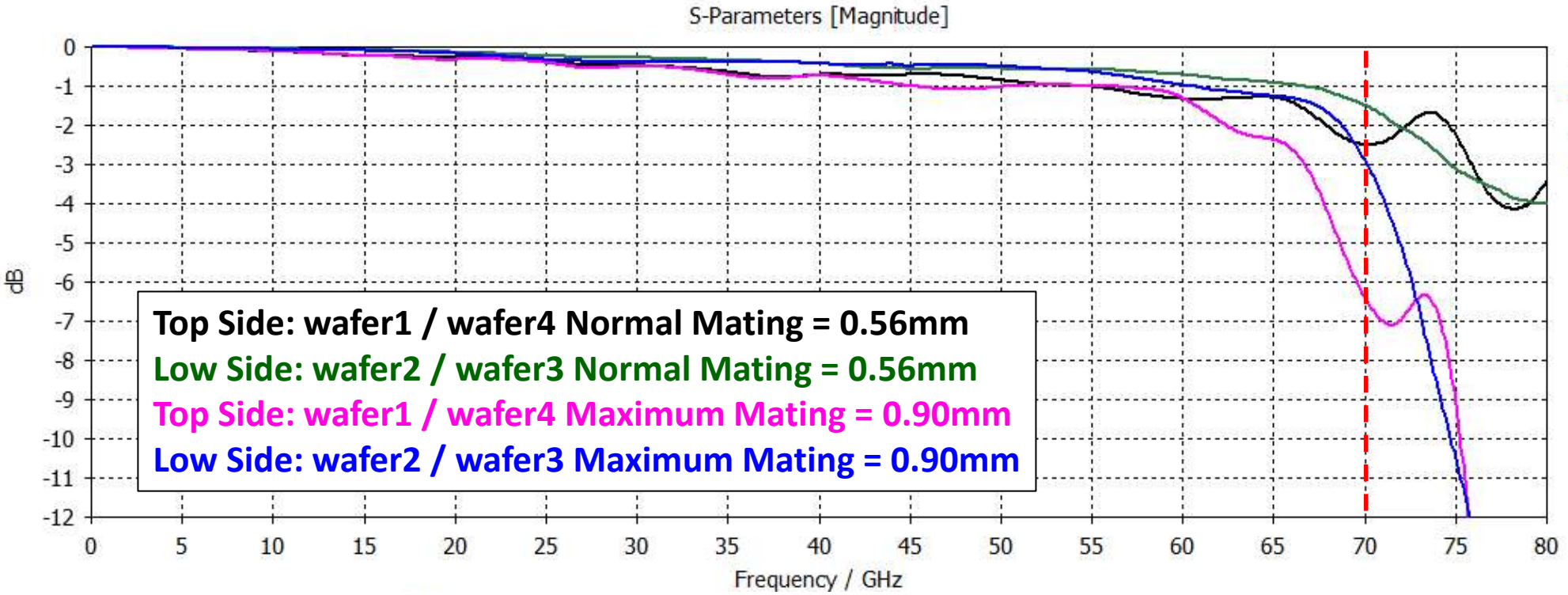
Line Card side			
wafer1		wafer4	
9	10	11	12
wafer2		wafer3	
13	14	15	16

Vertical OSFP-XD Connector Insertion Loss

Module side			
wafer1		wafer4	
1	2	3	4
wafer2		wafer3	
5	6	7	8

Line Card side			
wafer1		wafer4	
9	10	11	12
wafer2		wafer3	
13	14	15	16

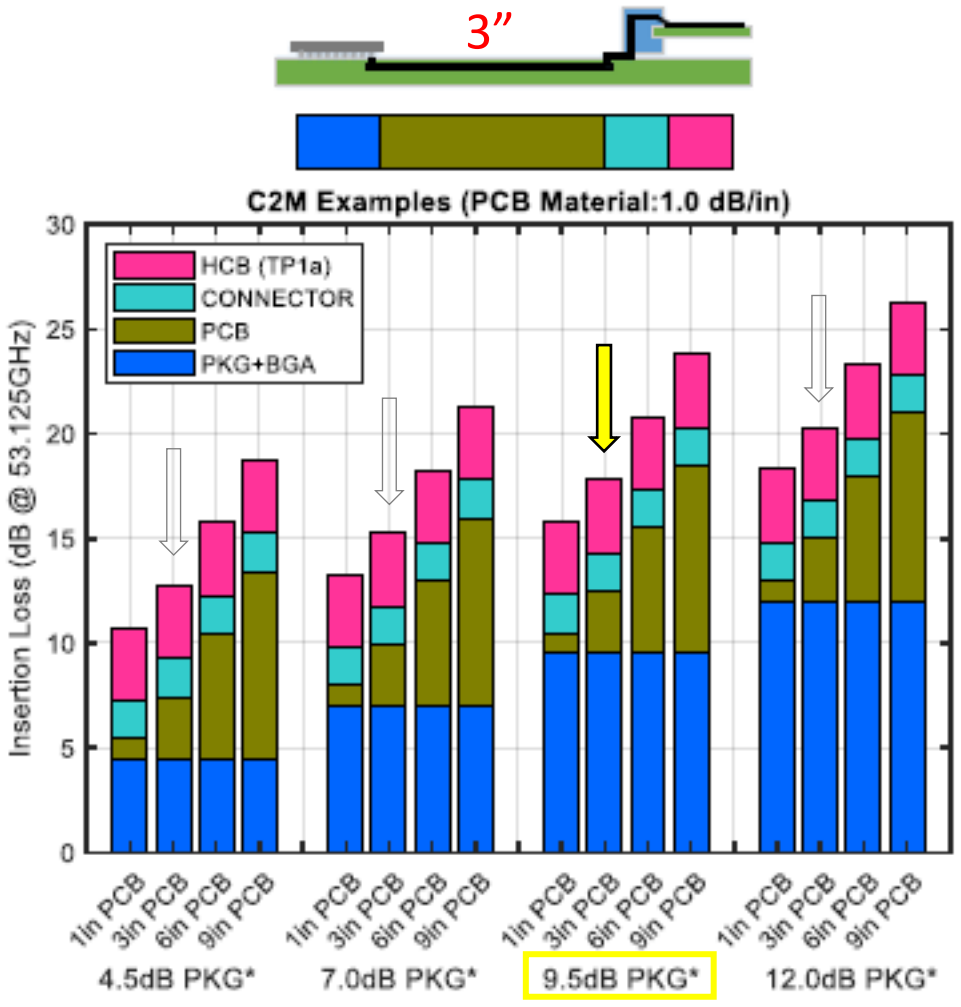
FEXT & NEXT in Appendix 3

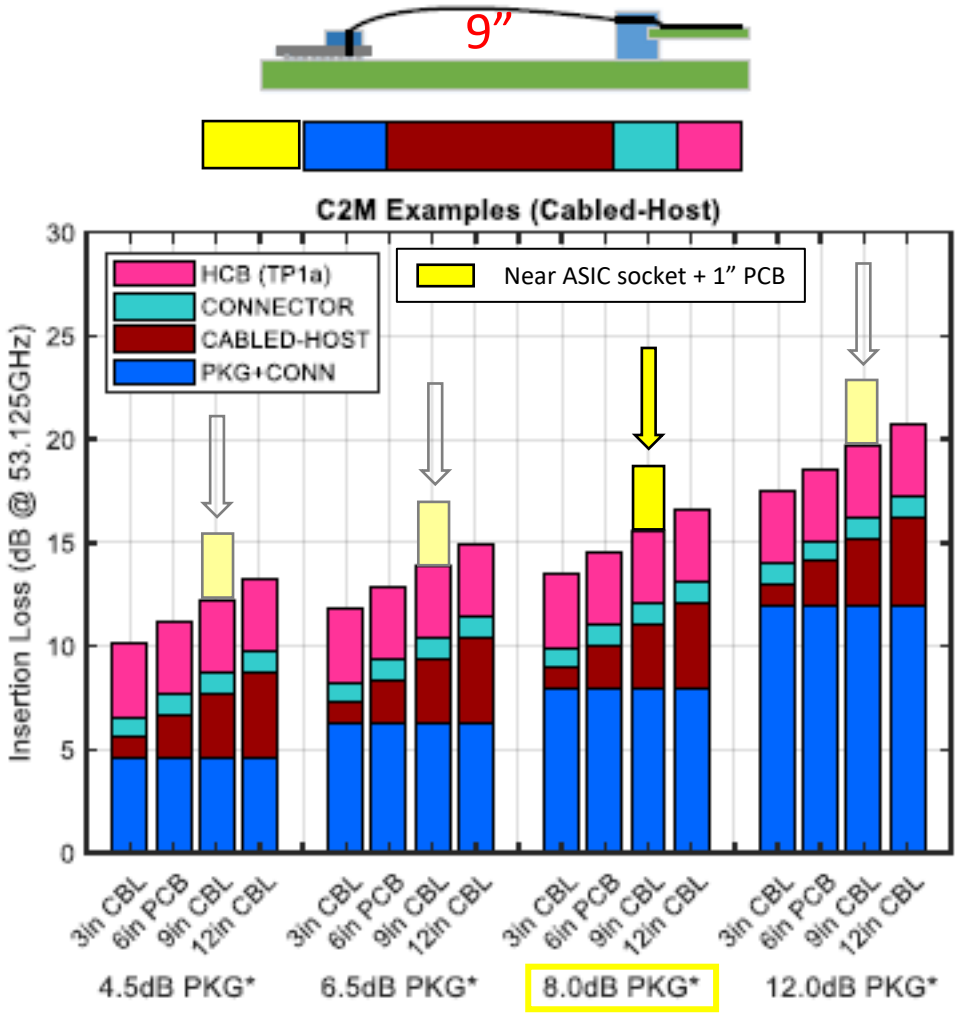


Outline

- Introduction
- Dual Front ASIC VLC Baseline
- Vertical OSFP Connector
- Vertical OSFP-XD Connector
- **➢ Stripline vs. Twinax Loss**
- Single Front ASIC VLC Alternatives
- Conclusions
- Appendix 1: PCIe
- Appendix 2: Vertical OSFP Connector FEXT & NEXT
- Appendix 3: Vertical OSFP-XD Connector FEXT & NEXT
- Appendix 4: Rack Power Limitations

224G PAM4 ASIC to Module Stripline vs. Twinax/PCB Link Loss



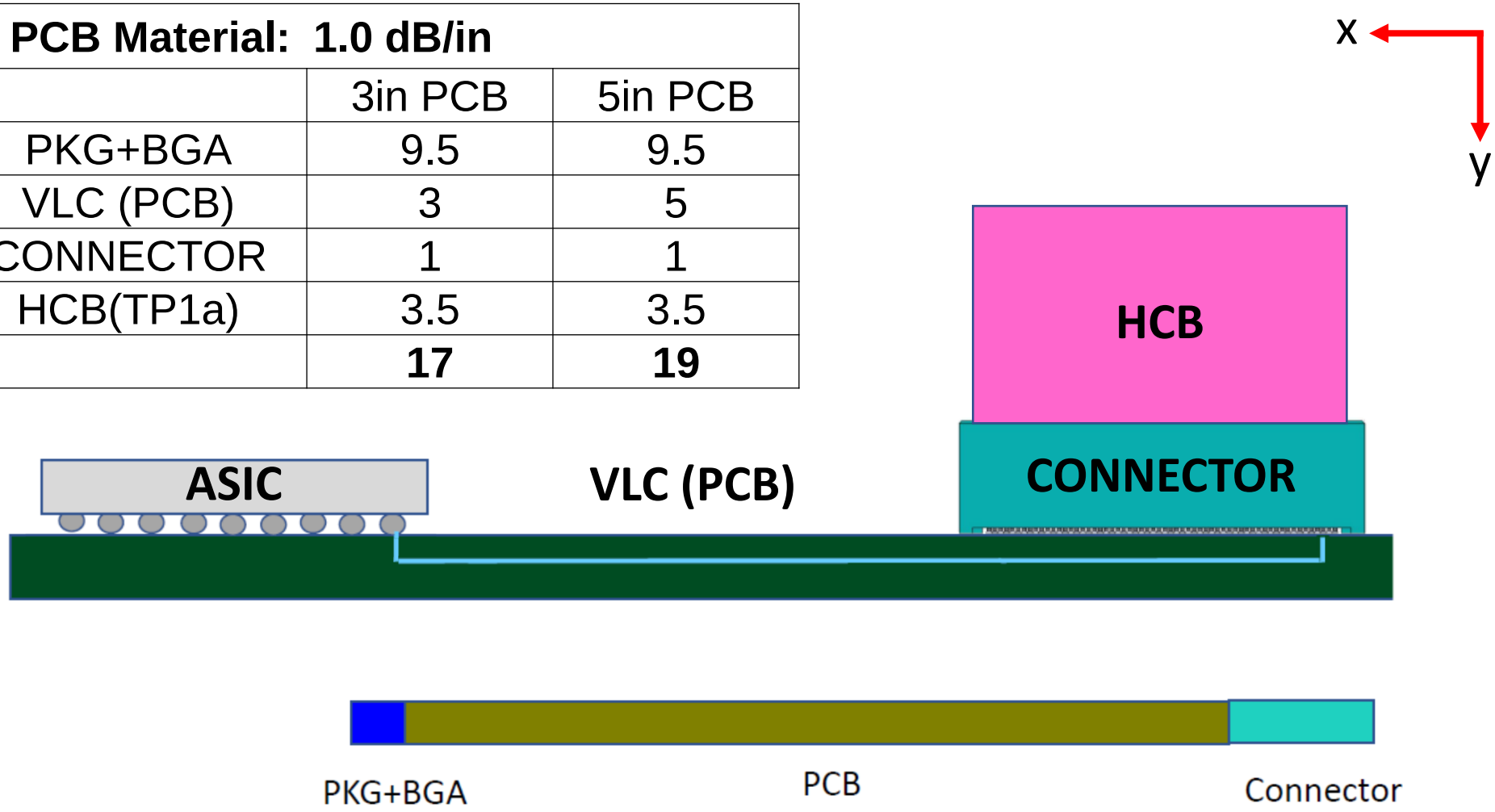


S. Kocis, Amphenol, N. Tracy, TE, 8/26/21, www.ieee802.org/3/B400G/public/21_08/kocsis_b400g_01a_210826.pdf

>9dB PKG: L. Ben-Artsi, Marvell, R. Mellitz, Samtec, www.ieee802.org/3/df/public/22_07/benartsi_3df_01a_2207.pdf

224G PAM4 ASIC to VLC Module Stripline Link Loss

PCB Material: 1.0 dB/in			
		3in PCB	5in PCB
	PKG+BGA	9.5	9.5
	VLC (PCB)	3	5
	CONNECTOR	1	1
	HCB(TP1a)	3.5	3.5
Total		**17**	**19**



Outline

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➢ **Single Front ASIC VLC Alternatives**

- Conclusions
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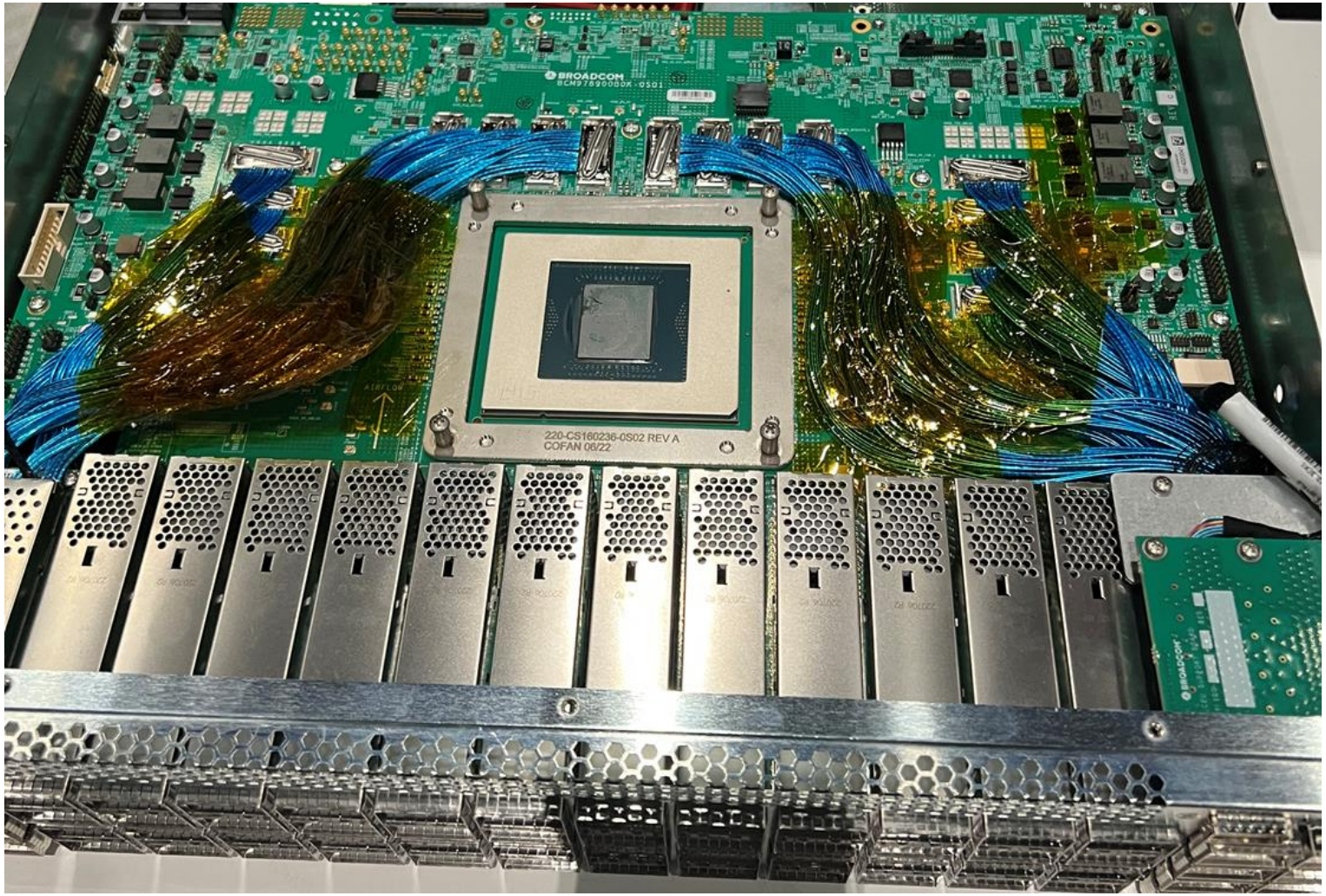
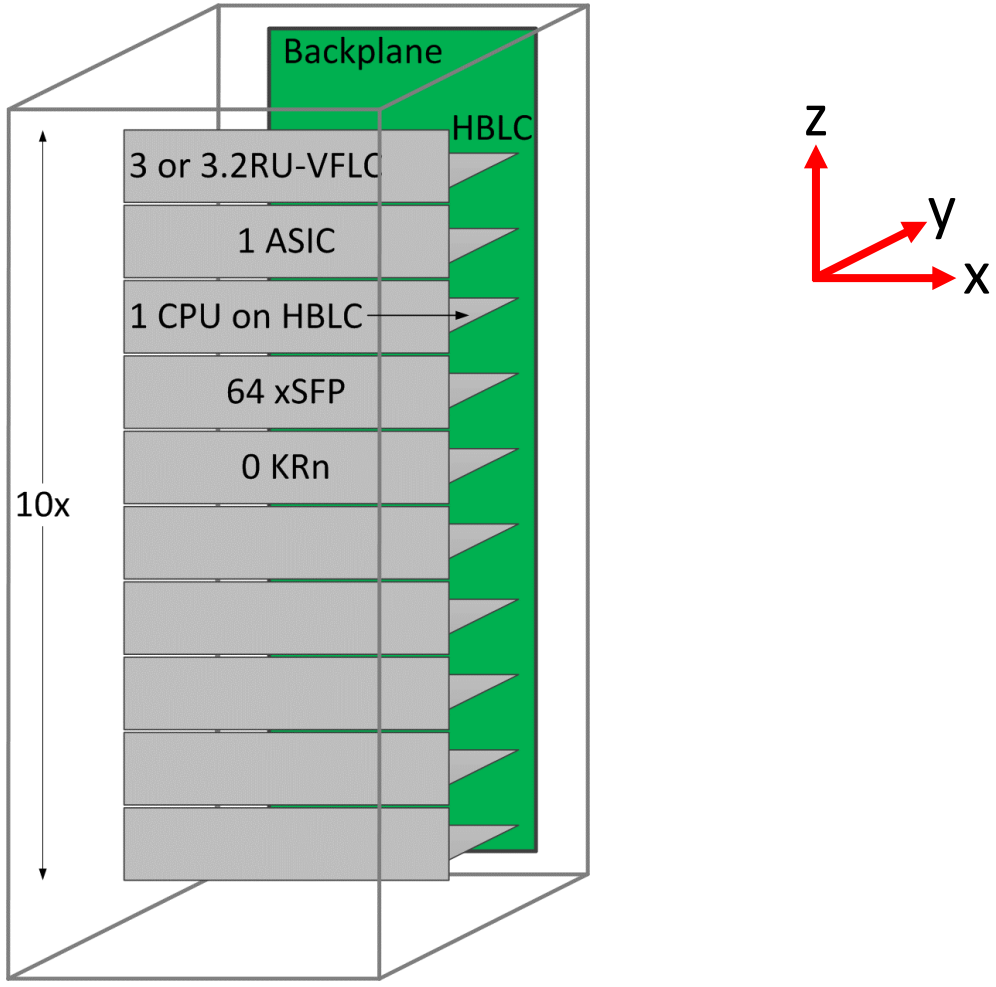
Broadcom 2RU-HLC, 64 OSFP, TH5 ASIC, Reference Design

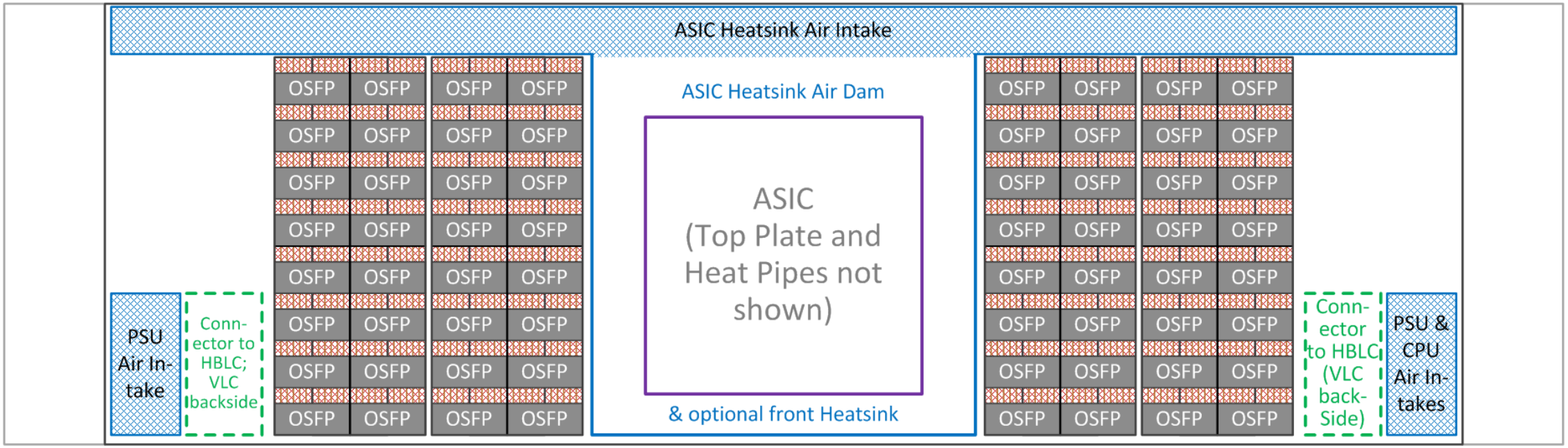


- 2RU-HLC 16x Rack
- Advantage:
  - PCB $L_{RF\text{-}MAX}$ = 5”
- Problems:
  - S.I. of stacked connectors
  - Obstruction of module air-flow
  - Assembly of Twinax cables
- Can we have the advantage without the problems?

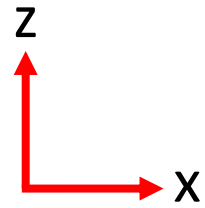
3.2RU-VLC 10x Rack



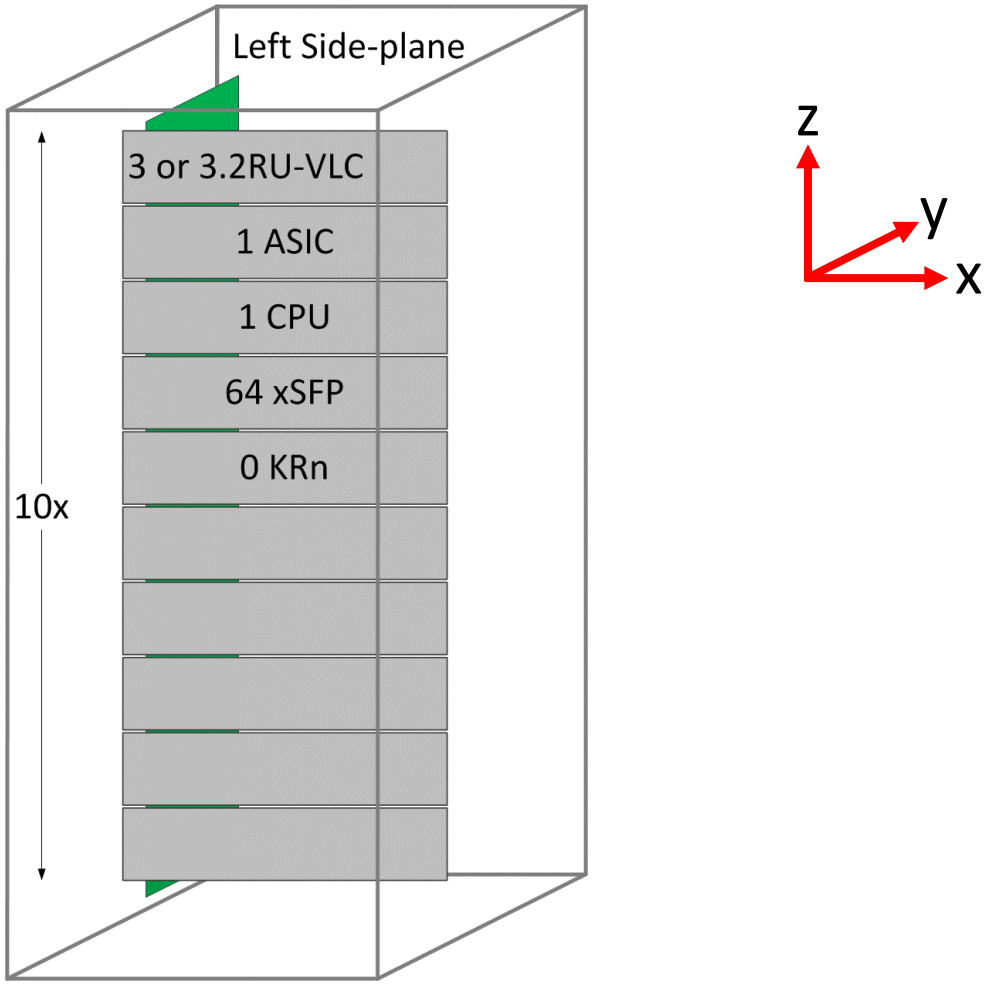
3.2RU-VLC, 64 OSFP, 1 ASIC, 5.2” $L_{RF\text{-}MAX}$ (Full Front View)



- OSFP vertical pitch = 15mm (per MSA)
  horizontal pitch = 24mm
- PCB Stripline $L_{RF\text{-}MAX}$ =
  120mm + 12mm = 132mm **(5.2")**

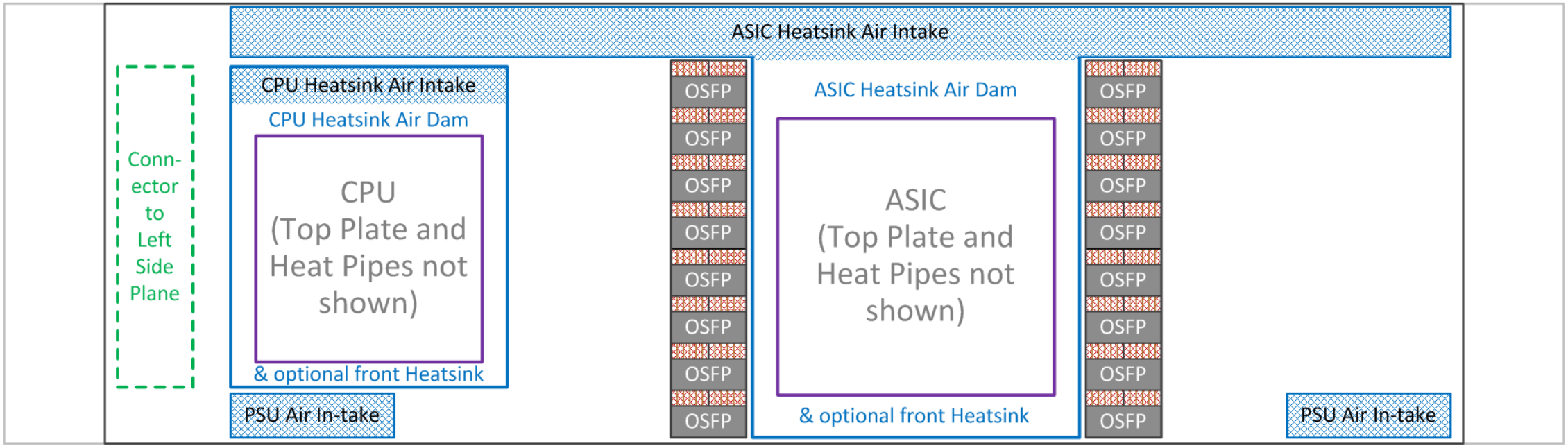


3.2RU-VLC Rack w/ Left Side-plane (No Backplane & No HBLC)

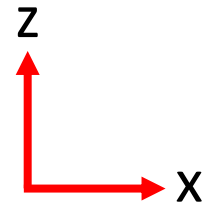


Right Side-plane is an equivalent alternative

3.2RU-VLC, 16 OSFP-HDA, 1 ASIC, 1 CPU, 2.0” $L_{RF\text{-}MAX}$ (Front View)



- PCB Stripline $L_{RF\text{-}MAX}$ = 39mm + 12mm = 51mm **(2.0")**
- HDA: High Density Array connector (ex. Interposer) for high count I/O
- ~30dB IL budget makes 448G PAM4 I/O feasible



Outline

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- Stripline vs. Twinax Loss
- Single Front ASIC VLC Alternative

➢ Conclusions

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- Appendix 2: Vertical OSFP Connector FEXT & NEXT
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- Appendix 4: Rack Power Limitations

HLC Optics vs. Vertical Line Card (VLC) Front Pluggable Optics

Optics		RF Type	$L_{RF\text{-}MAX}$	RF I/O Density
HLC	Front Pluggable (OSFP, QSFP)	Stripline in PCB	9” - 12”	1x
	Front Pluggable (OSFP, QSFP)	Twinax over PCB	9” - 12”	1x
	Assembled on PCB Near Package (NPO)	Stripline in PCB	3” - 4”	2x
VLC	Front Pluggable (OSFP, QSFP)	Stripline in PCB	3” - 4”	1x

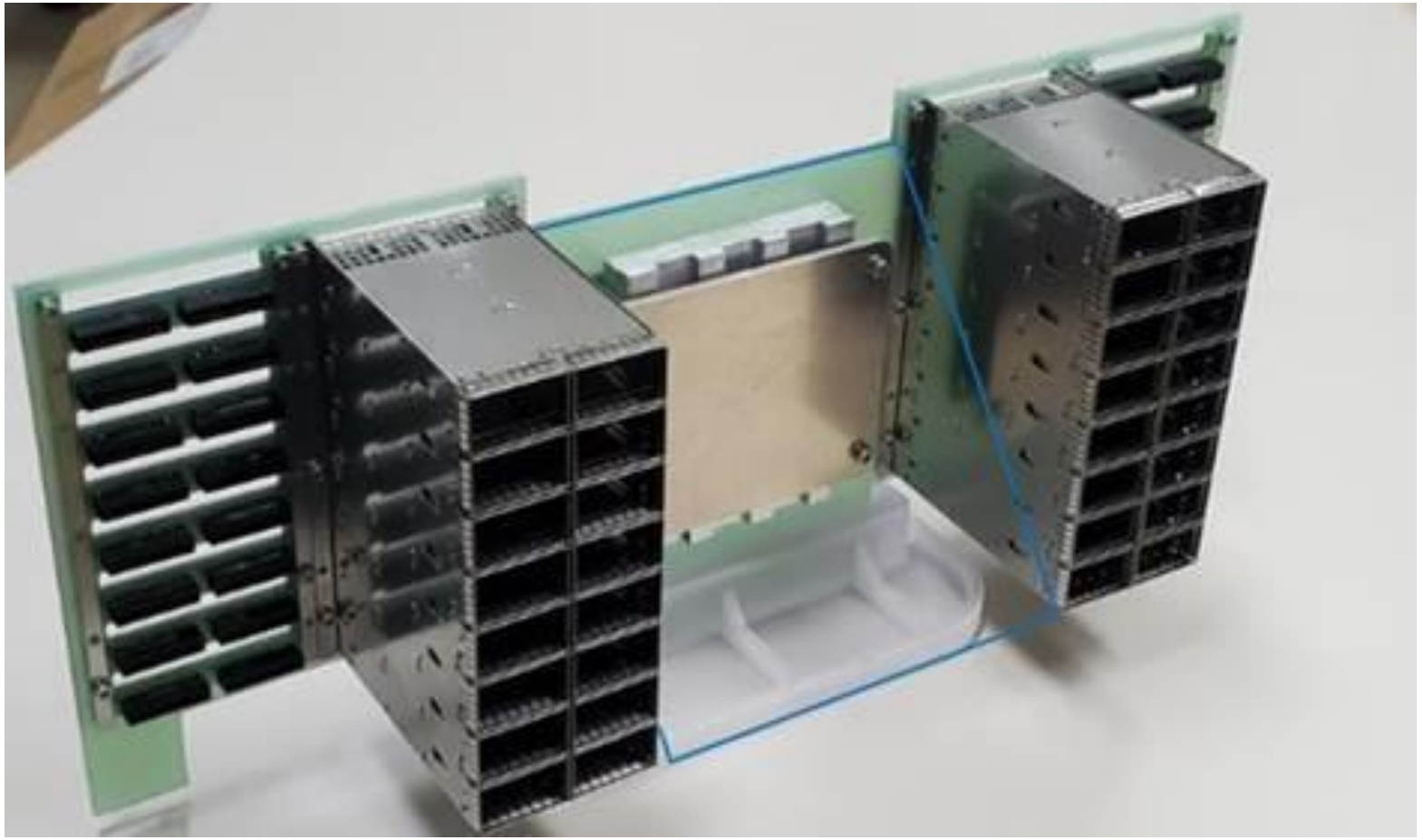
HLC Optics vs. Vertical Line Card (VLC) Front Pluggable Optics

Optics		RF Type	$L_{RF\text{-}MAX}$	RF I/O Density	Front Access	Air Flow Obstacles
HLC	Front Pluggable (OSFP, QSFP)	Stripline in PCB	9” - 12”	1x	Yes	Cage & Connector
	Front Pluggable (OSFP, QSFP)	Twinax over PCB	9” - 12”	1x	Yes	Cables & Connector
	Assembled on PCB Near Package (NPO)	Stripline in PCB	3” - 4”	2x	No	ASIC & other NPOs
VLC	Front Pluggable (OSFP, QSFP)	Stripline in PCB	3” - 4”	1x	Yes	None

HLC Optics vs. Vertical Line Card (VLC) Front Pluggable Optics

Optics		RF Type	$L_{RF\text{-}MAX}$	RF I/O Density	Front Access	Air Flow Obstacles	Mature Tech.	Cost
HLC	Front Pluggable (OSFP, QSFP)	Stripline in PCB	9” - 12”	1x	Yes	Cage & Connector	Yes	1x
	Front Pluggable (OSFP, QSFP)	Twinax over PCB	9” - 12”	1x	Yes	Cables & Connector	No	>2x
	Assembled on PCB Near Package (NPO)	Stripline in PCB	3” - 4”	2x	No	ASIC & other NPOs	No	>1x
VLC	Front Pluggable (OSFP, QSFP)	Stripline in PCB	3” - 4”	1x	Yes	None	Yes	1x

VLC Demo in Yamaichi Booth 738



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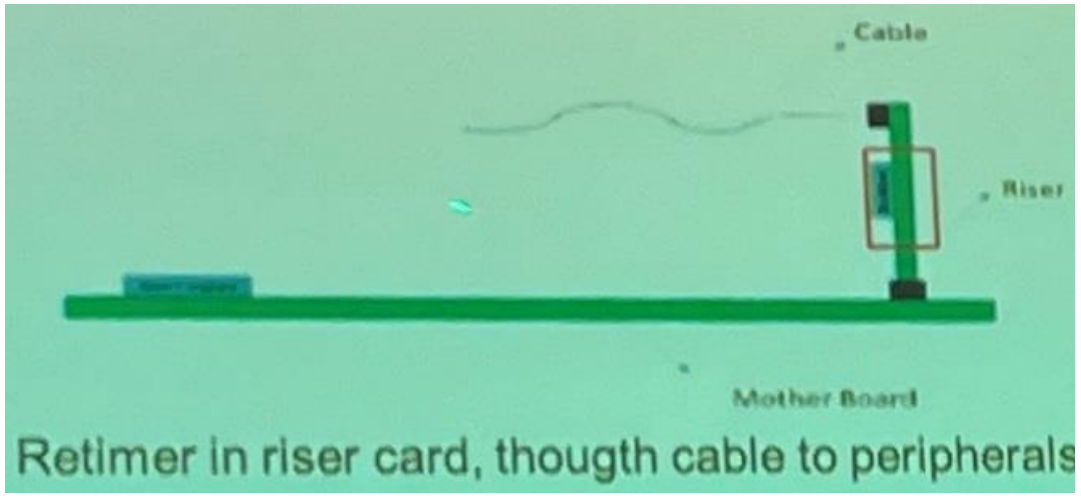
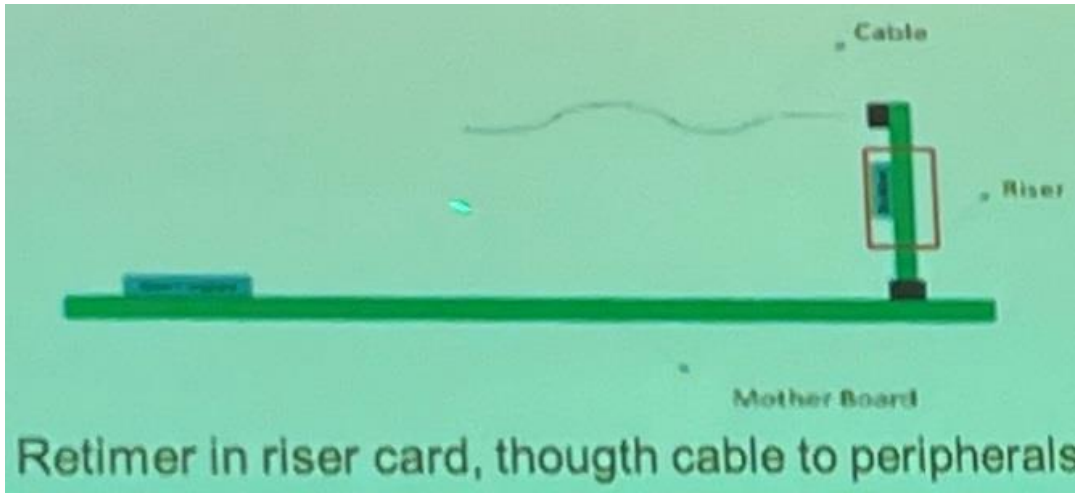
PCIe 6.0 External Connector w/ Re-timer on Riser



DesignCon 2023 Panel:
PCIe 6.0: Challenges of Achieving 64GT/s with PAM4 in Lossy, HVM Channels
1/31/23, 4:45 – 6:00PM
From presentation by Madhumita Sanyal, Sr. Mngr. Synopsys

Vertical OSFP-XD as PCIe External Connector w/ Retimer



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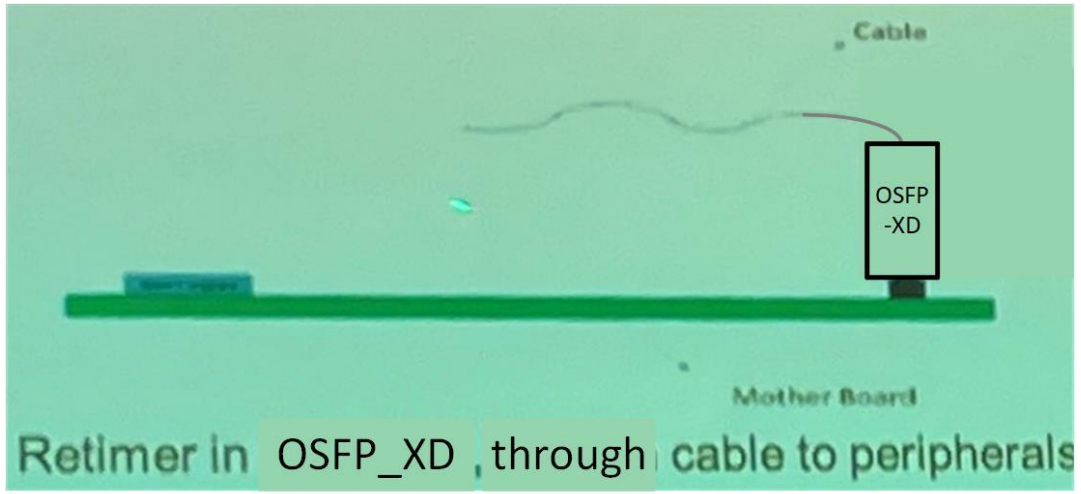


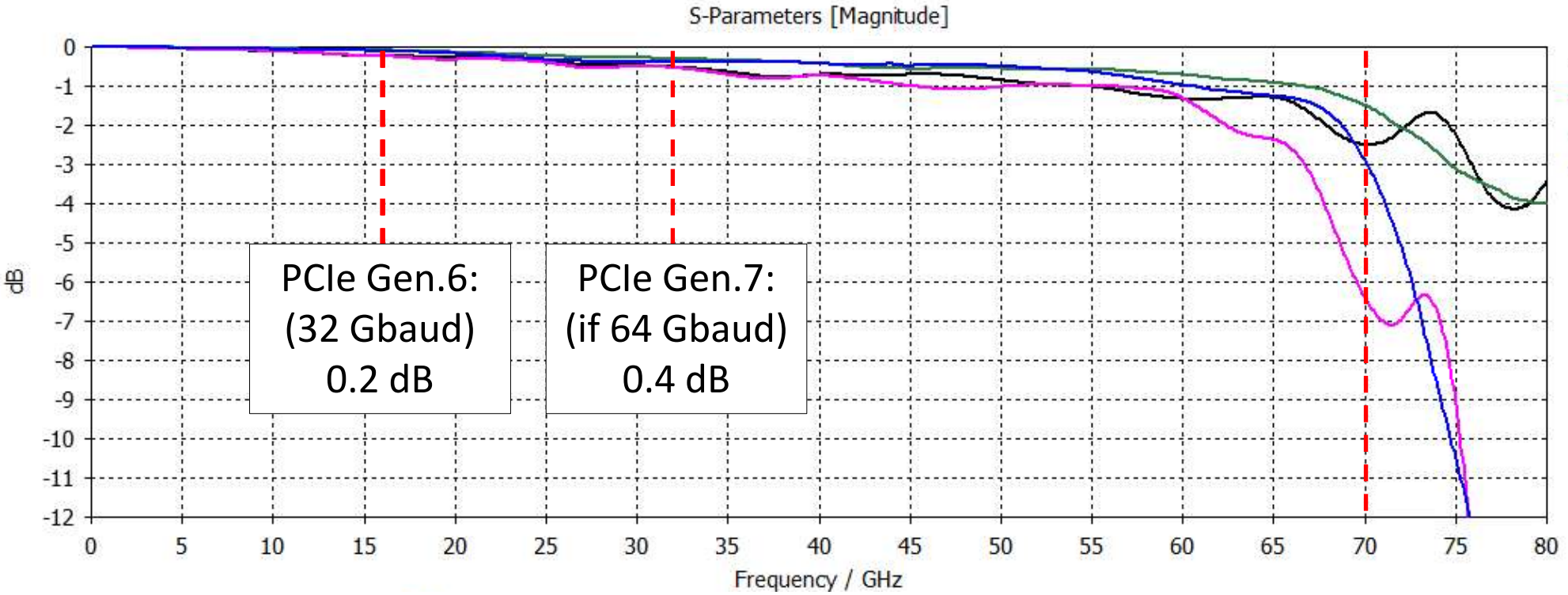
From proposal by Chris Cole to be made to OSFP-XD Ad Hoc (part of OSFP MSA)

Vertical OSFP-XD as PCIe External Connector Insertion Loss

Module side			
wafer1		wafer4	
1	2	3	4
wafer2		wafer3	
5	6	7	8

Line Card side			
wafer1		wafer4	
9	10	11	12
wafer2		wafer3	
13	14	15	16

Top Side: wafer1 / wafer4 Normal Mating = 0.56mm
Low Side: wafer2 / wafer3 Normal Mating = 0.56mm
Top Side: wafer1 / wafer4 Maximum Mating = 0.90mm
Low Side: wafer2 / wafer3 Maximum Mating = 0.90mm



Example 16x112G PAM4 AEC (or ACC) for Ethernet Applications

Credo

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➢ **Appendix 2: Vertical OSFP Connector FEXT & NEXT**

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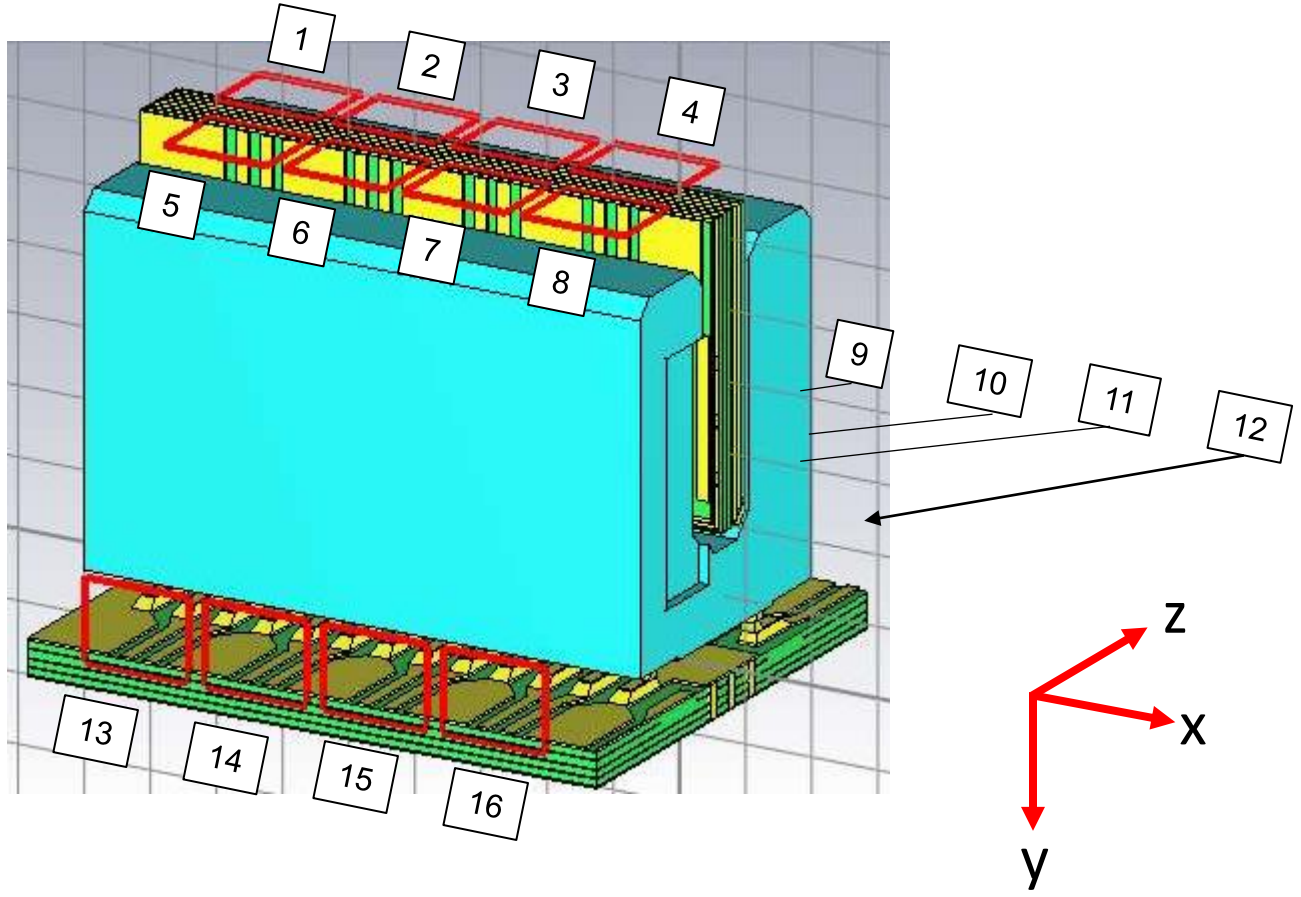
Vertical OSFP Connector Simulation Model

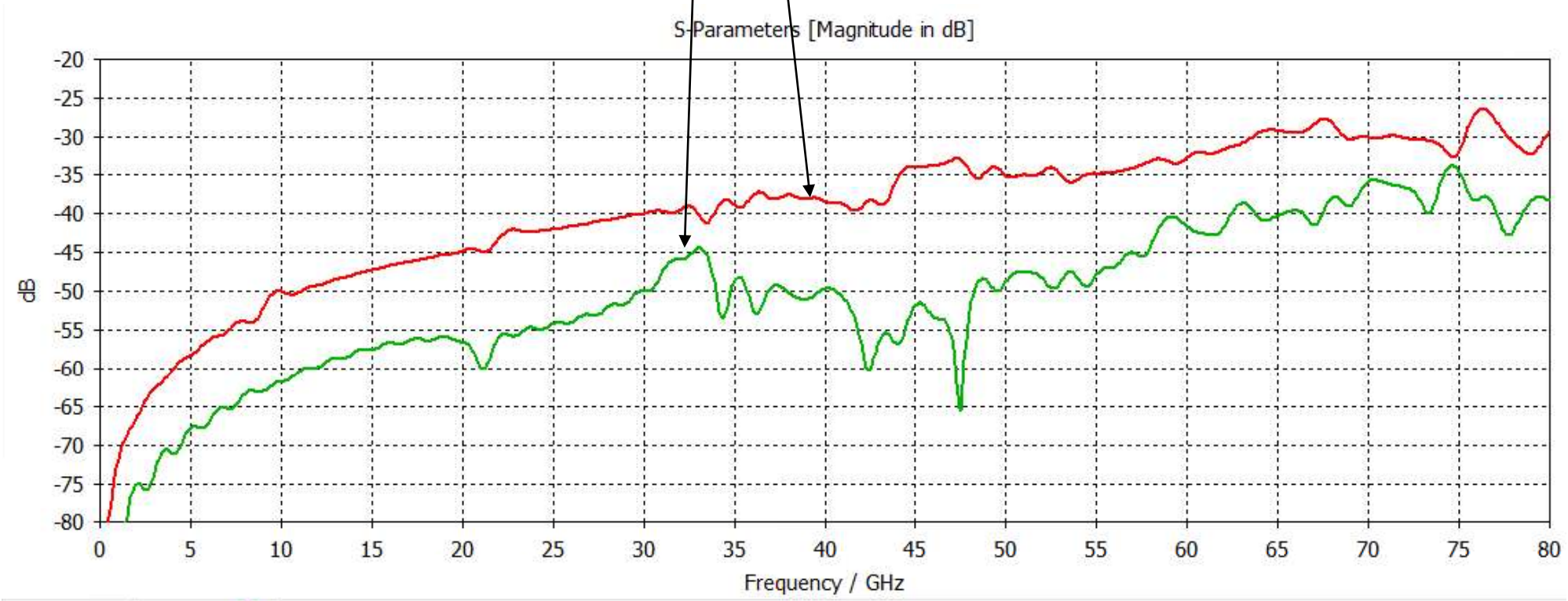


Vertical OSFP Connector FEXT 0.56mm Normal Mating

Module side			
Front			
1	2	3	4
Back			
5	6	7	8

Line Card side			
Front			
9	10	11	12
Back			
13	14	15	16

Victim

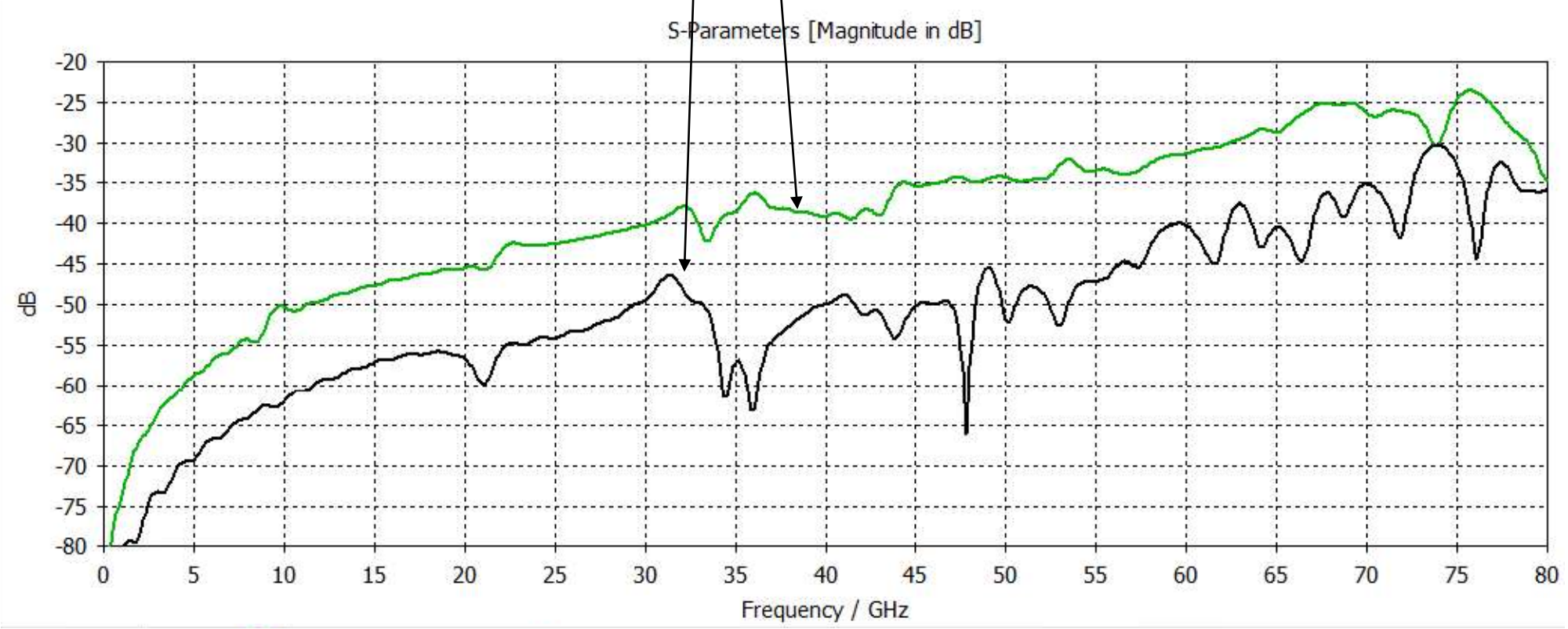


Vertical OSFP Connector FEXT 0.90mm Max Mating

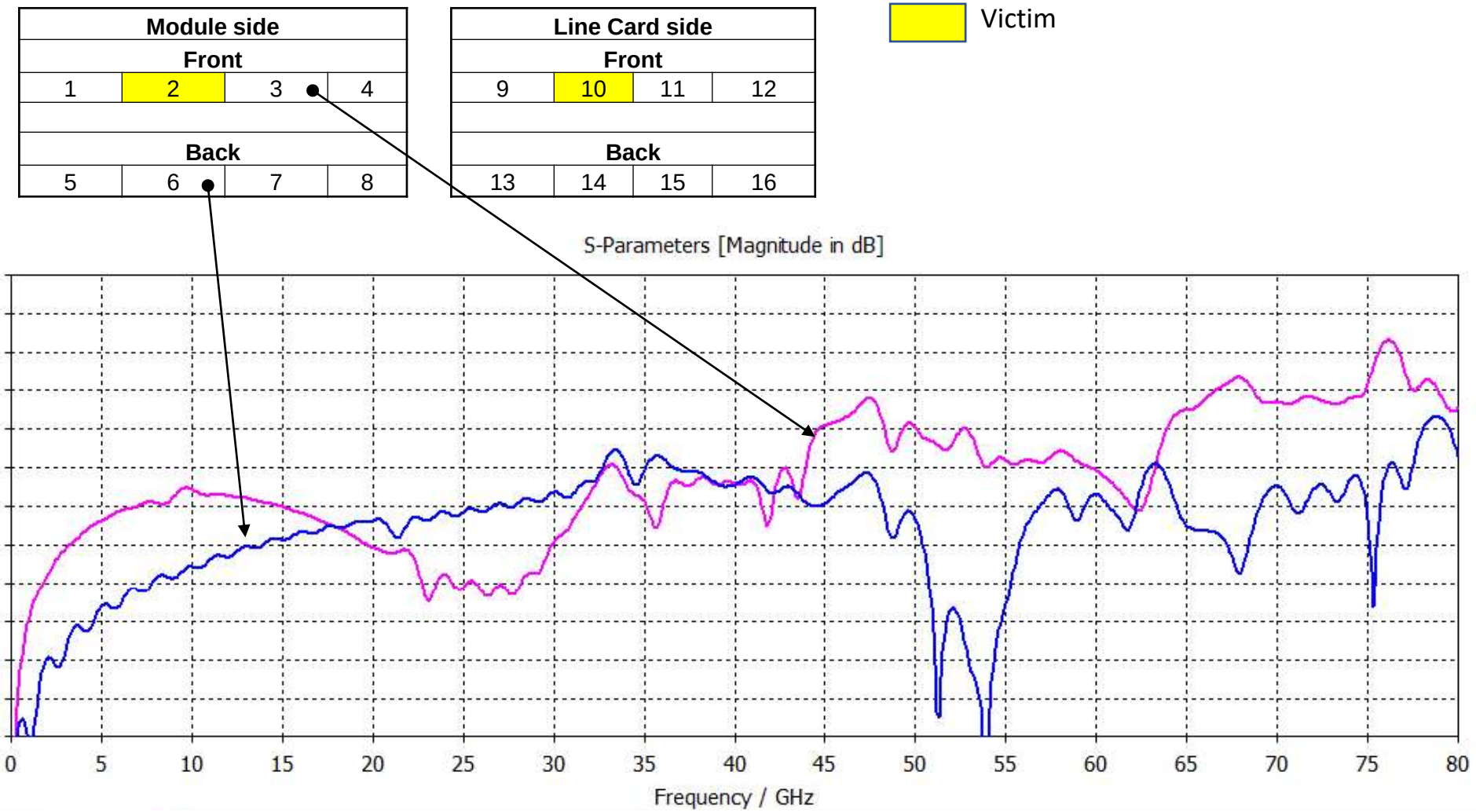
Module side			
Front			
1	2	3	4
Back			
5	6	7	8

Line Card side			
Front			
9	10	11	12
Back			
13	14	15	16

Victim



Vertical OSFP Connector NEXT 0.56mm Normal Mating



Vertical OSFP Connector NEXT 0.90mm Max Mating

Module side			
Front			
1	2	3	4
Back			
5	6	7	8

Line Card side			
Front			
9	10	11	12
Back			
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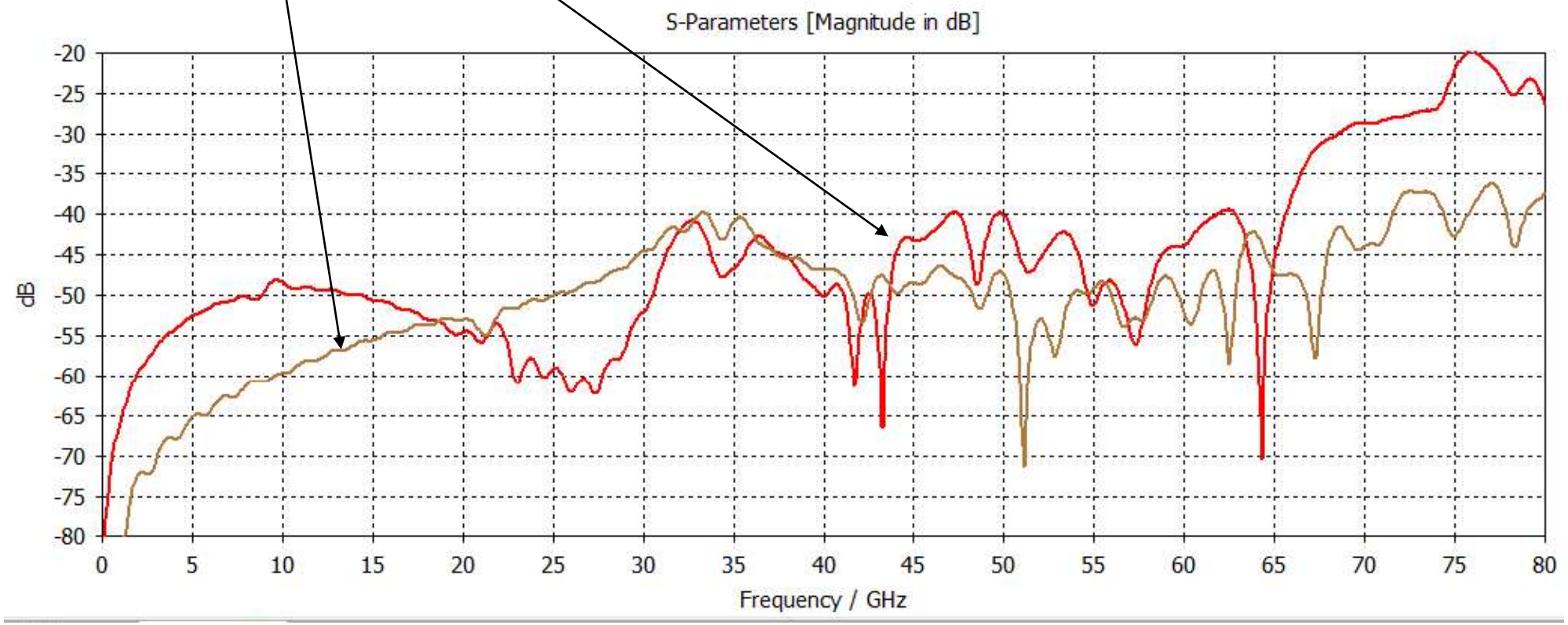
Victim



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➢ **Appendix 3: Vertical OSFP-XD Connector FEXT & NEXT**

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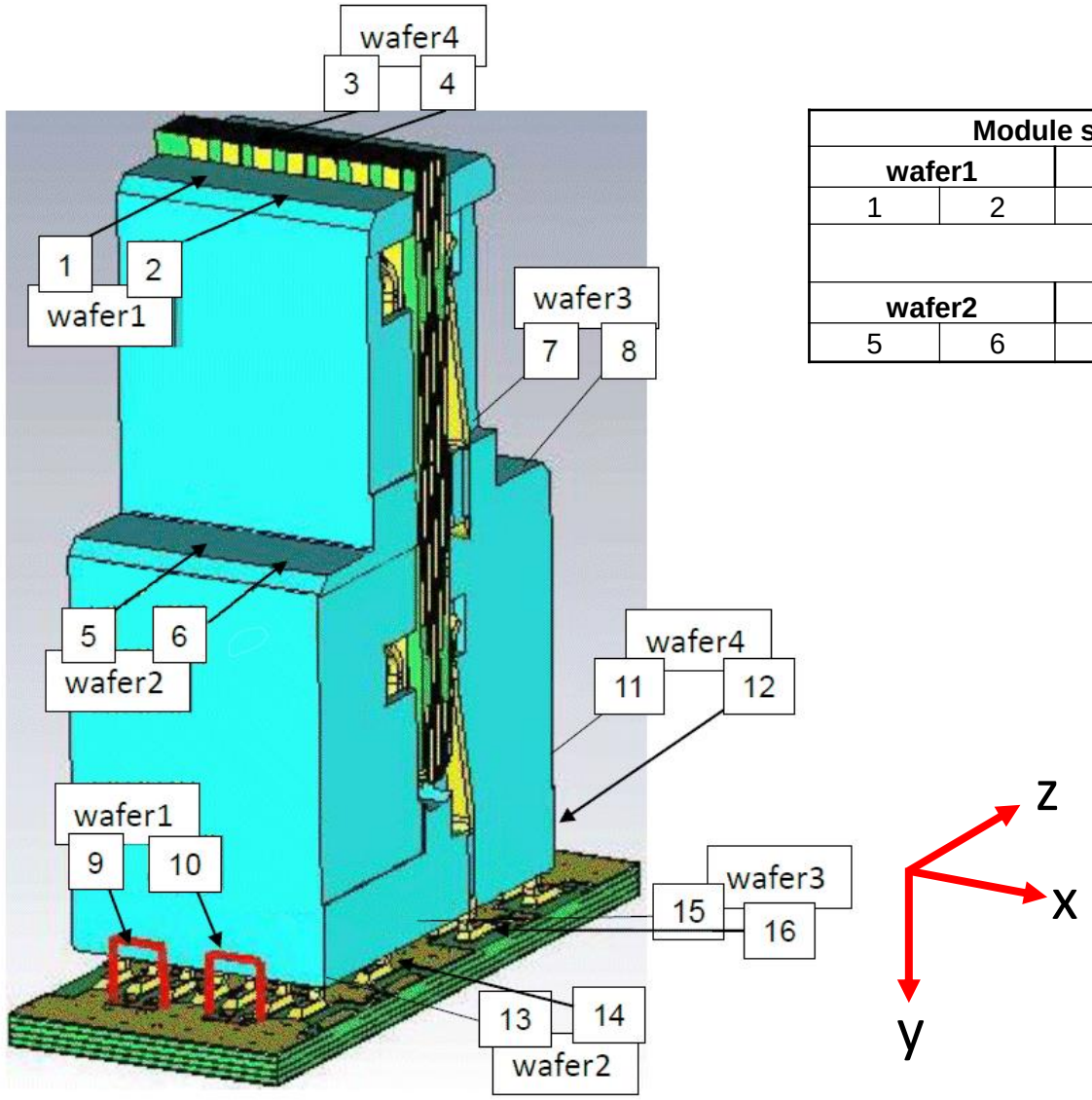
Vertical OSFP-XD Connector Simulation Model



Module side			
wafer1		wafer4	
1	2	3	4
wafer2		wafer3	
5	6	7	8

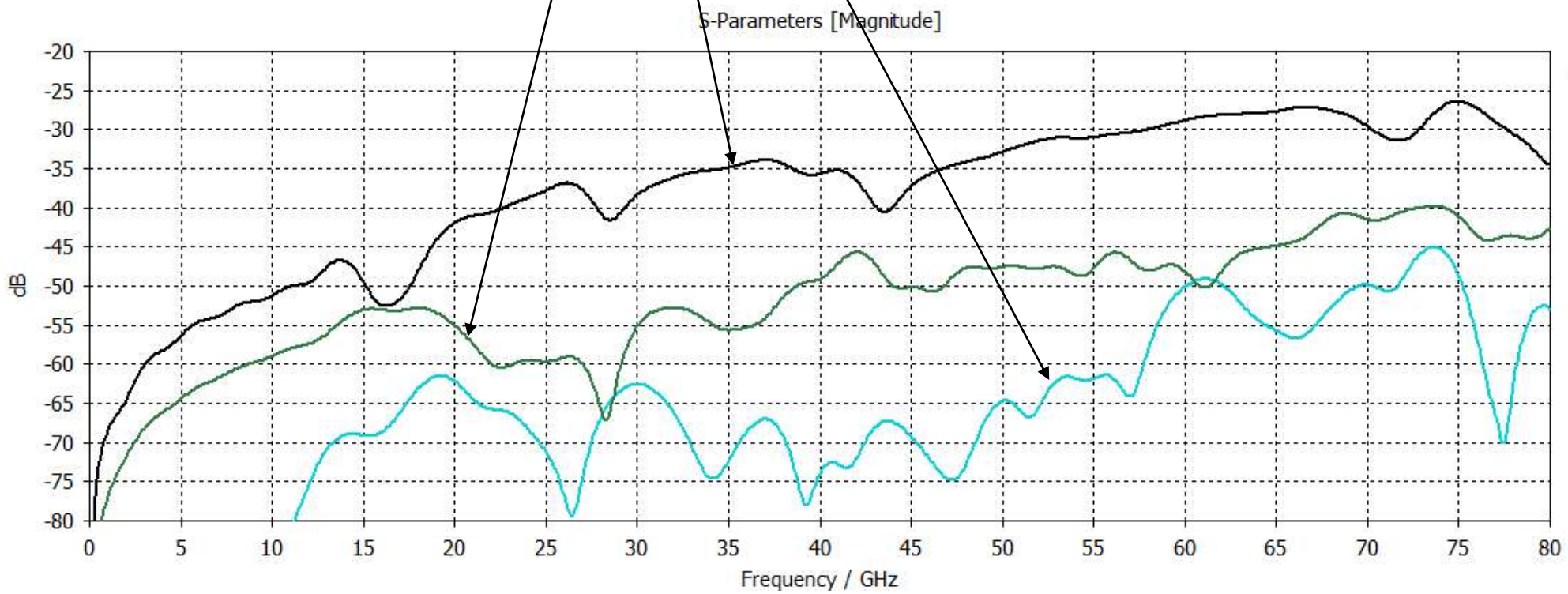
Line Card side			
wafer1		wafer4	
9	10	11	12
wafer2		wafer3	
13	14	15	16

Vertical OSFP-XD Connector FEXT 0.56mm Normal Mating

Module side			
Top Side			
wafer1		wafer4	
1	2	3	4
Low Side			
wafer2		wafer3	
5	6	7	8

Line Card side			
Top Side			
wafer1		wafer4	
9	10	11	12
Low Side			
wafer2		wafer3	
13	14	15	16

Victim



Vertical OSFP-XD Connector FEXT 0.56mm Normal Mating

Module side			
Top Side			
wafer1		wafer4	
1	2	3	4
Low Side			
wafer2		wafer3	
5	6	7	8

Line Card side			
Top Side			
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Low Side			
wafer2		wafer3	
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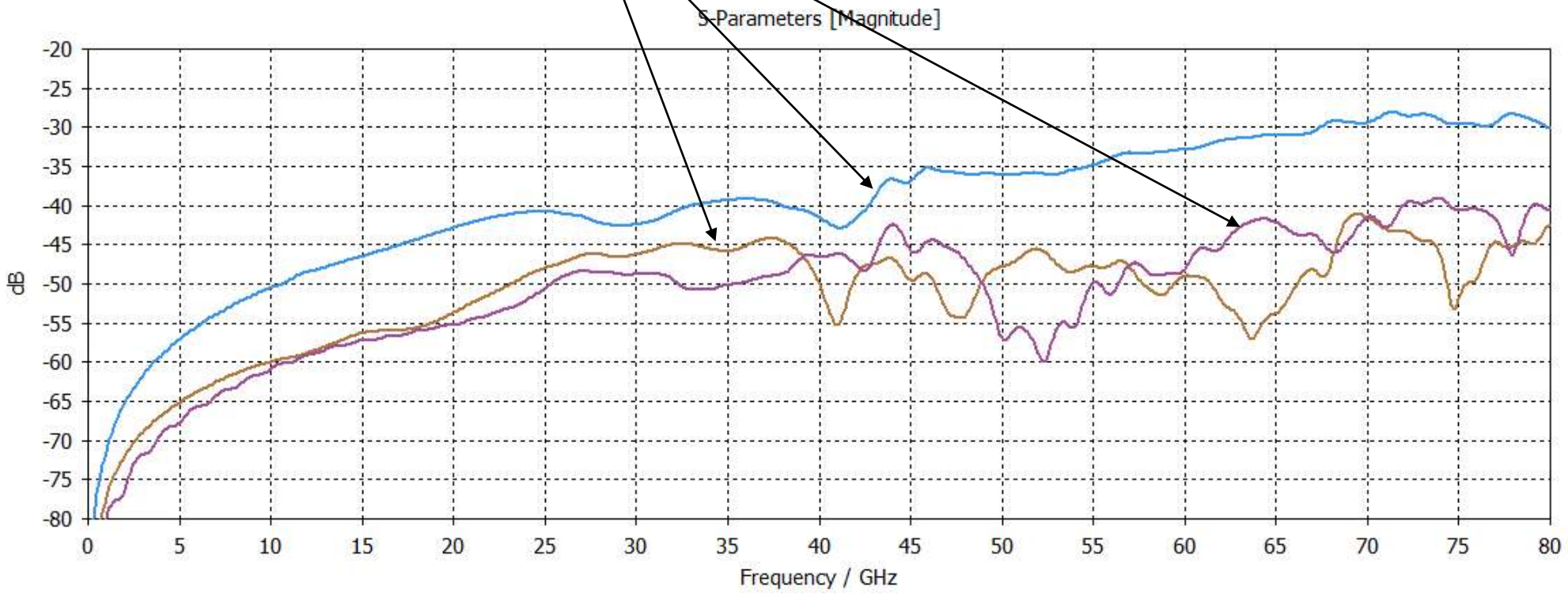
Victim



Vertical OSFP-XD Connector FEXT 0.90mm Max Mating

Module side			
Top Side			
wafer1		wafer4	
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Line Card side			
Top Side			
wafer1		wafer4	
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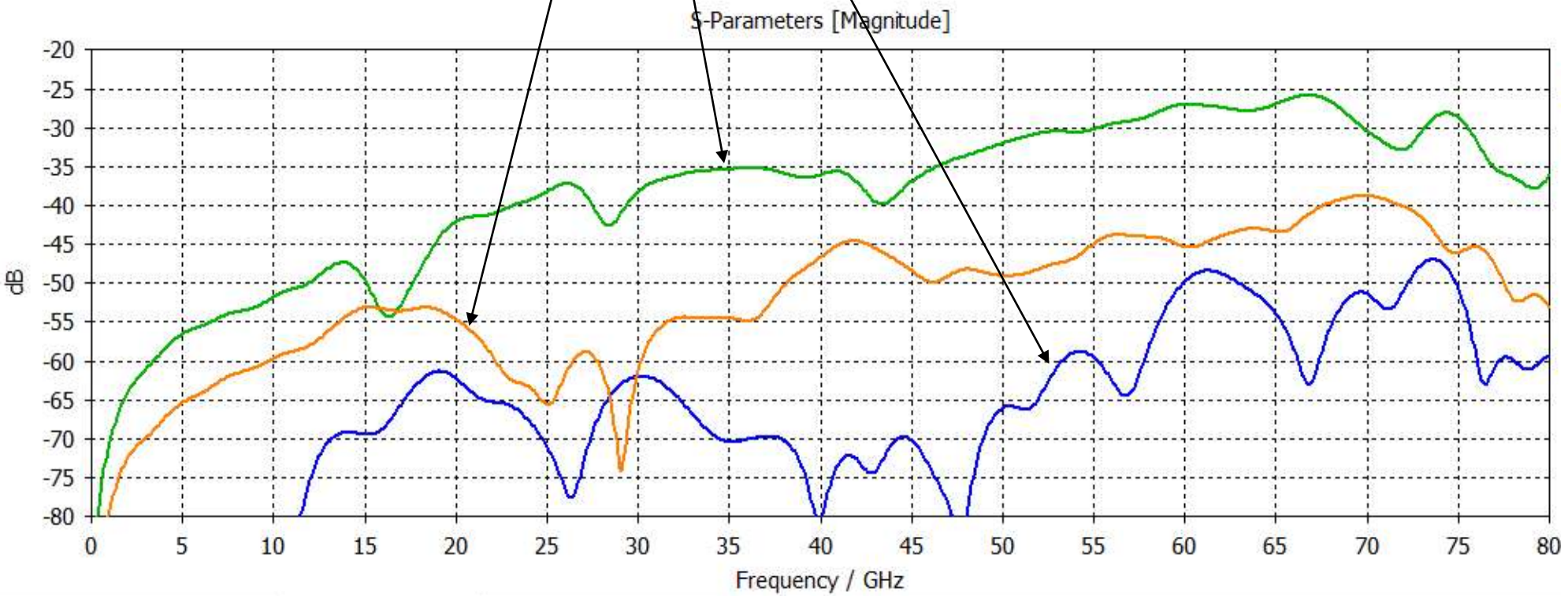
Low Side			
wafer2		wafer3	
13	14	15	16

Victim



Vertical OSFP-XD Connector FEXT 0.90mm Max Mating

Module side			
Top Side			
wafer1		wafer4	
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Line Card side			
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wafer2		wafer3	
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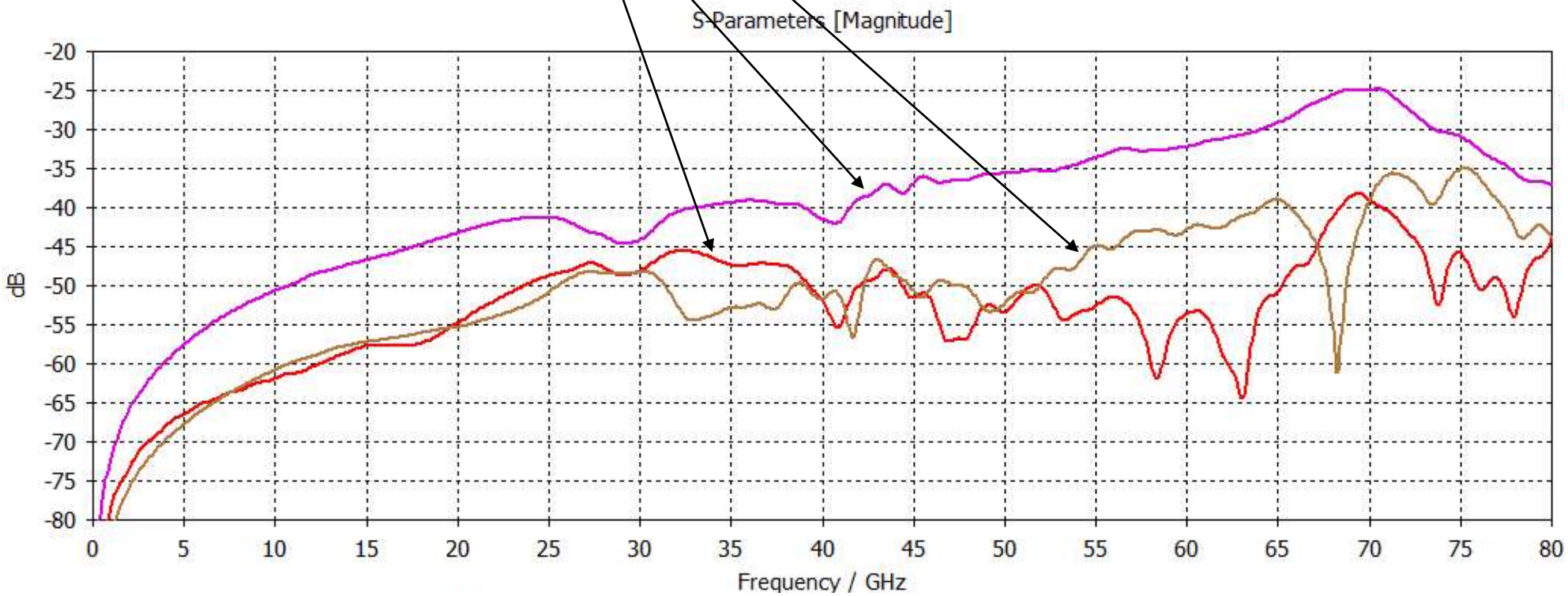
Victim

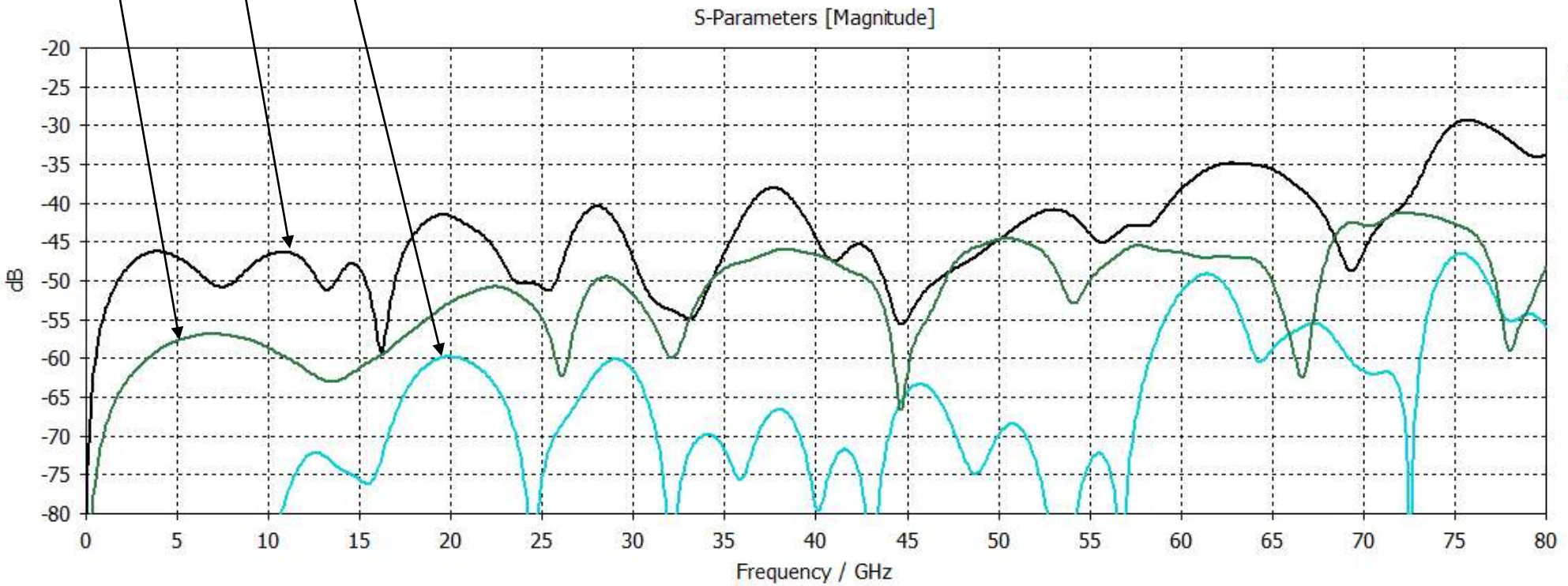


Vertical OSFP-XD Connector NEXT 0.56mm Normal Mating

Module side			
Top Side			
wafer1		wafer4	
1	2	3	4
Low Side			
wafer2		wafer3	
5	6	7	8

Line Card side			
Top Side			
wafer1		wafer4	
9	10	11	12
Low Side			
wafer2		wafer3	
13	14	15	16

Victim

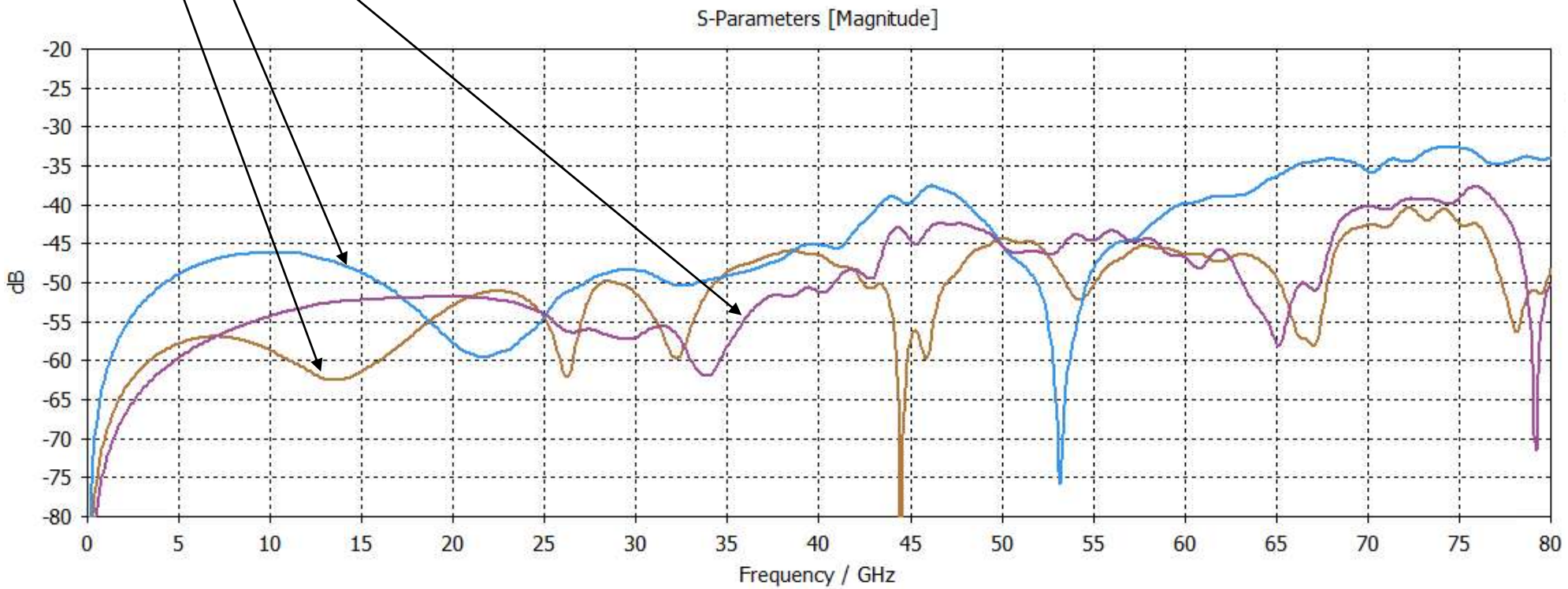


Vertical OSFP-XD Connector NEXT 0.56mm Normal Mating

Module side			
Top Side			
wafer1		wafer4	
1	2	3	4
Low Side			
wafer2		wafer3	
5	6	7	8

Line Card side			
Top Side			
wafer1		wafer4	
9	10	11	12
Low Side			
wafer2		wafer3	
13	14	15	16

Victim

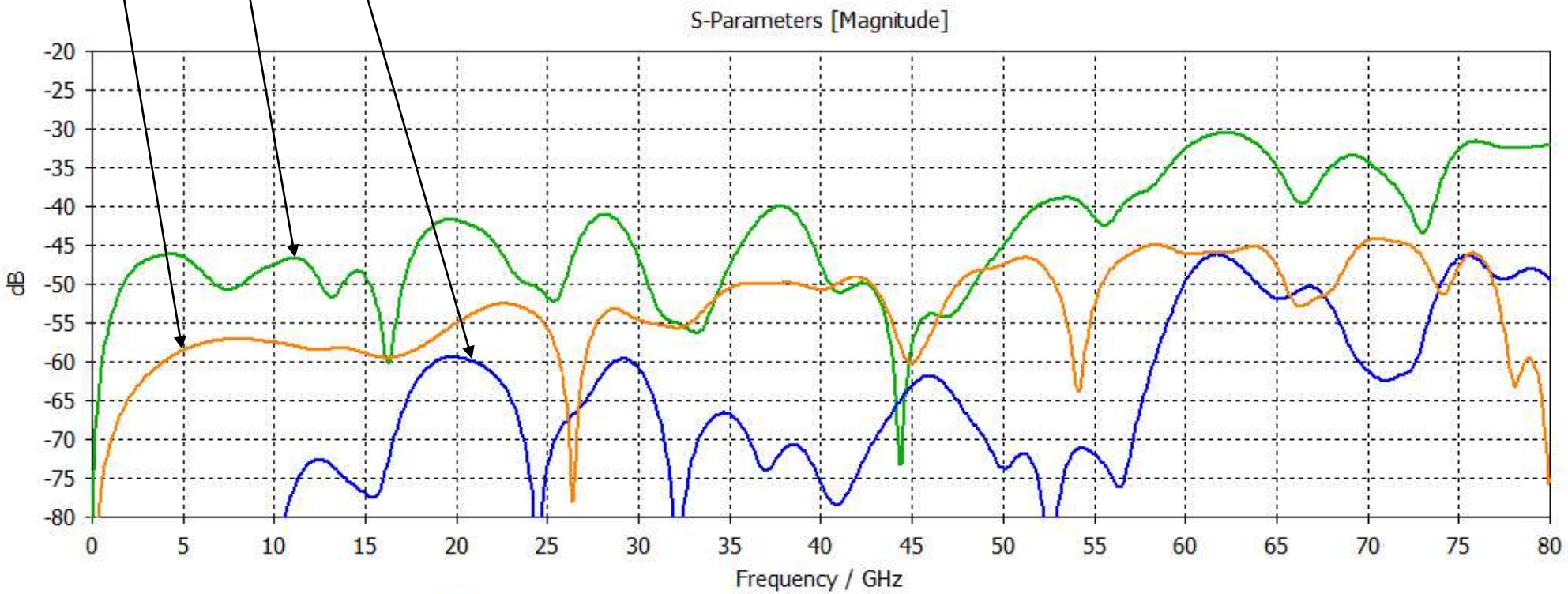


Vertical OSFP-XD Connector NEXT 0.90mm Max Mating

Module side			
Top Side			
wafer1		wafer4	
1	2	3	4
Low Side			
wafer2		wafer3	
5	6	7	8

Line Card side			
Top Side			
wafer1		wafer4	
9	10	11	12
Low Side			
wafer2		wafer3	
13	14	15	16

Victim

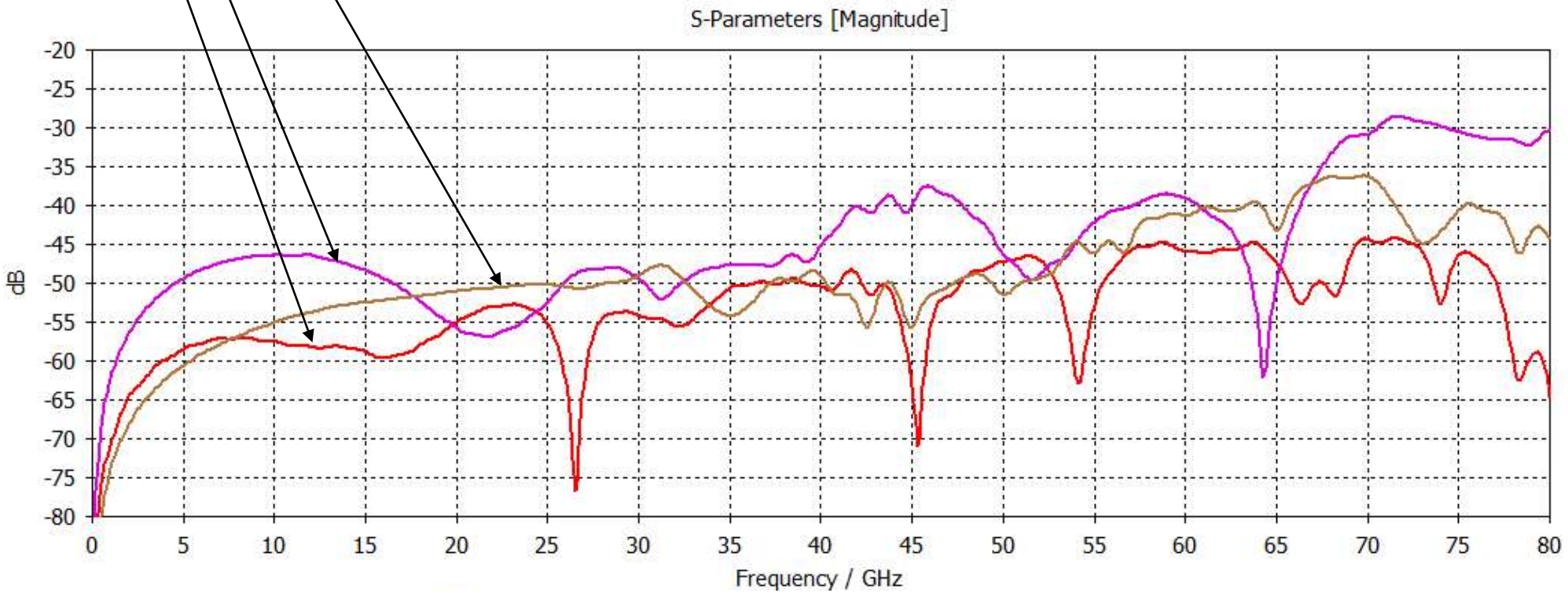


Vertical OSFP-XD Connector NEXT 0.90mm Max Mating

Module side			
Top Side			
wafer1		wafer4	
1	2	3	4
Low Side			
wafer2		wafer3	
5	6	7	8

Line Card side			
Top Side			
wafer1		wafer4	
9	10	11	12
Low Side			
wafer2		wafer3	
13	14	15	16

Victim

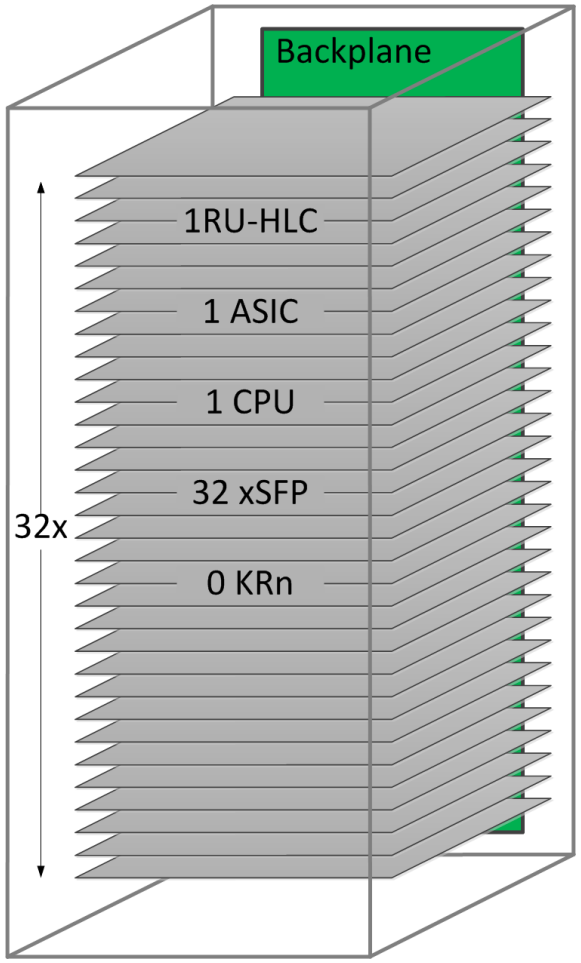


Outline

- Introduction
- Dual Front ASIC VLC Baseline
- Vertical OSFP Connector
- Vertical OSFP-XD Connector
- Stripline vs. Twinax Loss
- Single Front ASIC VLC Alternative
- Conclusions
- Appendix 1: PCIe
- Appendix 2: Vertical OSFP Connector FEXT & NEXT
- Appendix 3: Vertical OSFP-XD Connector FEXT & NEXT

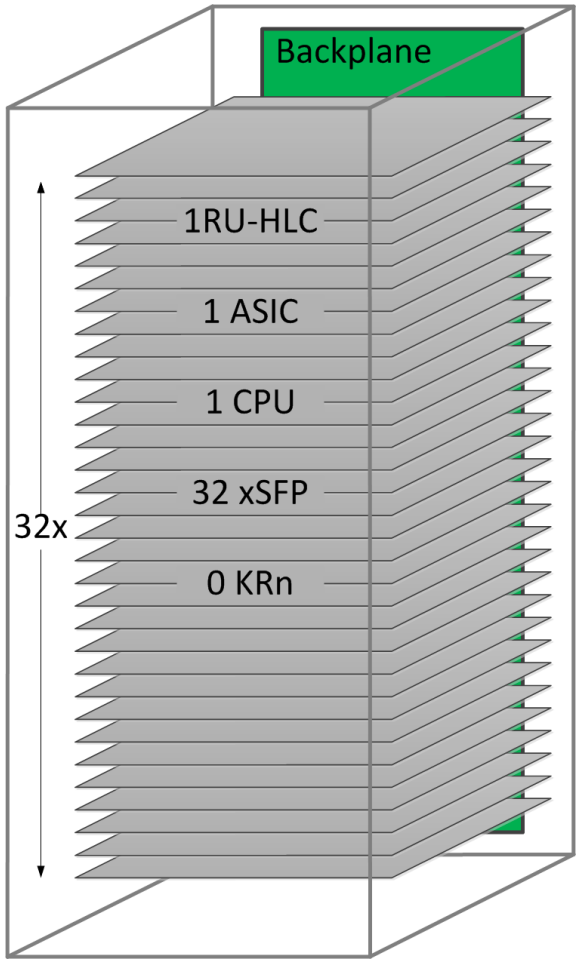
➢ **Appendix 4: Rack Power Limitations**

Ex.1: 12.8T ASIC HLC Racks



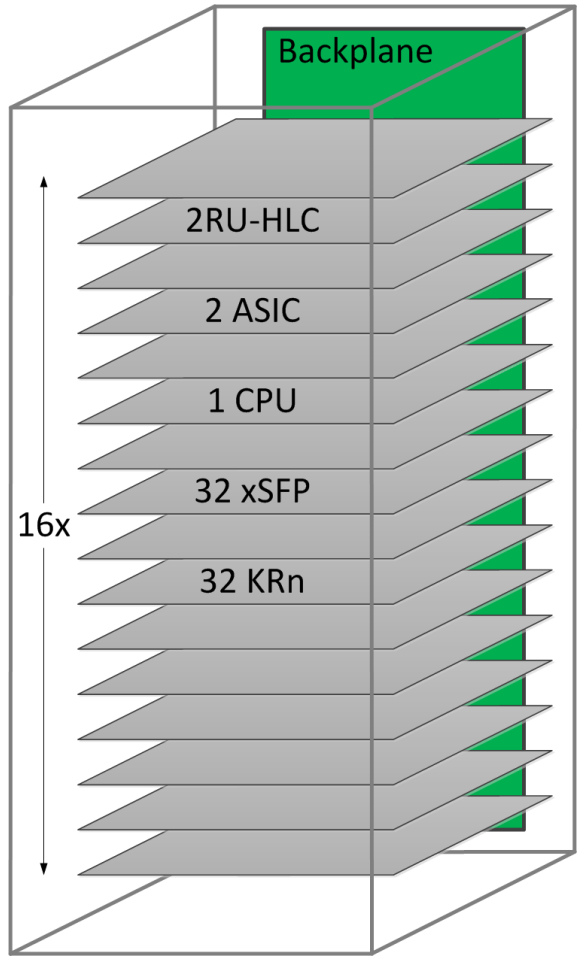
- 12.8T 1RU-HLC w/ 1x TH3 ASIC
- 32x 2x200G OSFPs (50G I/O)
- No Backplane links
- 1000W HLC (1200W OCP HLC)
- 32x Rack: 32KW

Ex.1: 12.8T ASIC HLC Racks



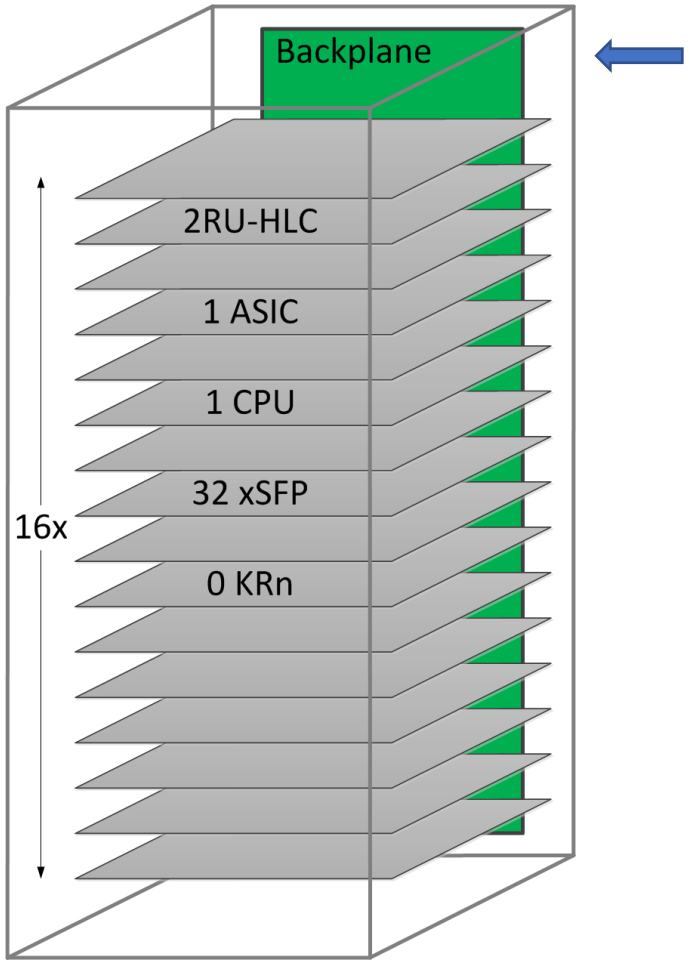
- 12.8T 1RU-HLC w/ 1x TH3 ASIC
- 32x 2x200G OSFPs (50G I/O)
- No Backplane links
- 1000W HLC (1200W OCP HLC)
- 32x Rack: 32KW

- 25.6T 2RU-HLC w/ 2x TH3 ASICs
- 32x 2x200G OSFPs (50G I/O)
- 32x 4x100G Backplane links
- 1950W HLC
- 16x Rack: 31KW



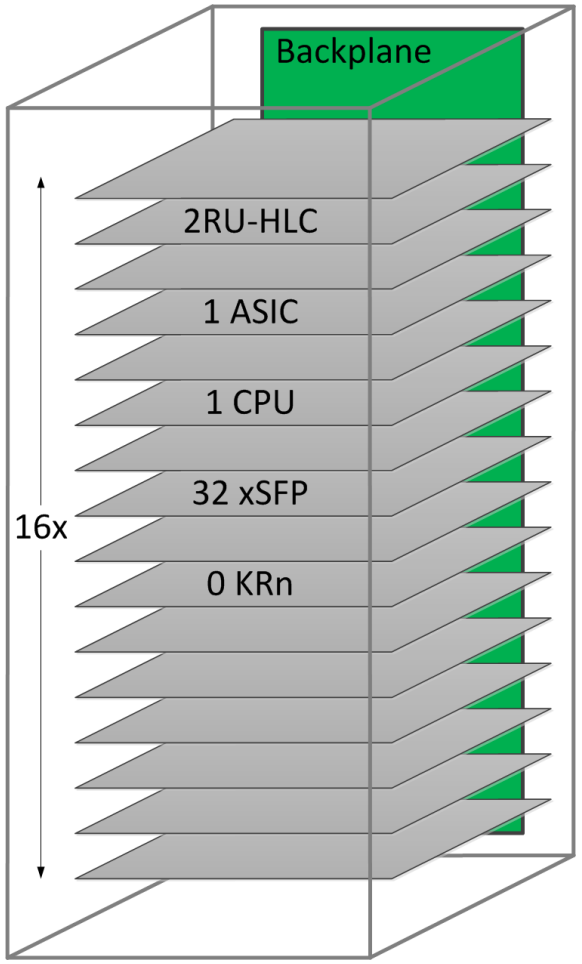
Fabric application

Ex.2: 25.6T ASIC HLC Racks



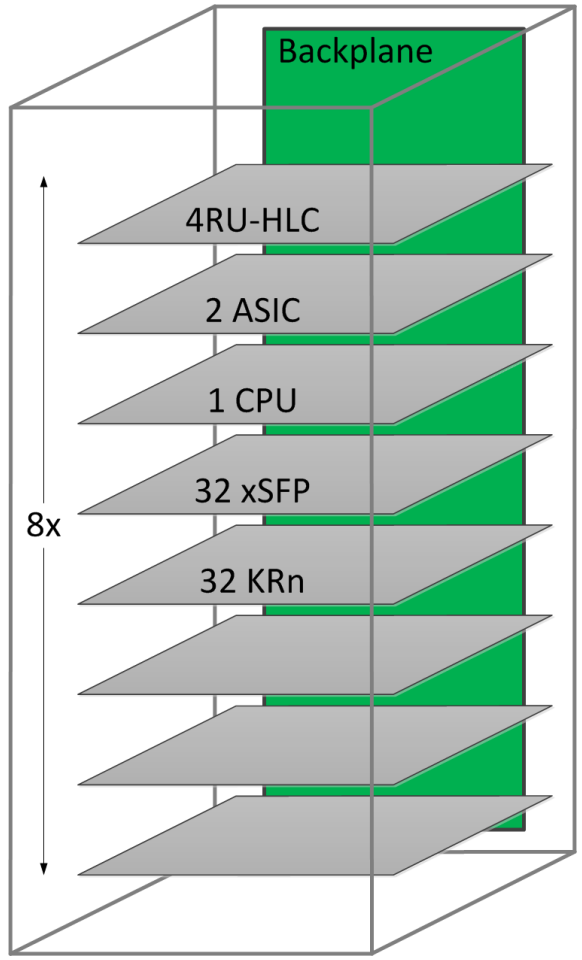
- 25.6T 2RU-HLC w/ 1x TH4 ASIC
- 32x 2x400G OSFPs (100G I/O)
- No Backplane links
- 1750W HLC
- 16x Rack: 28KW

Ex.2: 25.6T ASIC HLC Racks



- 25.6T 2RU-HLC w/ 1x TH4 ASIC
- 32x 2x400G OSFPs (100G I/O)
- No Backplane links
- 1750W HLC
- 16x Rack: 28KW

- 51.2T 4RU-HLC w/ 2x TH4 ASICs
- 32x 2x400G OSFPs (100G I/O)
- 32x 8x100G Backplane links
- 3400W HLC
- 8x Rack: 27KW



Fabric application

Line Card Component Power

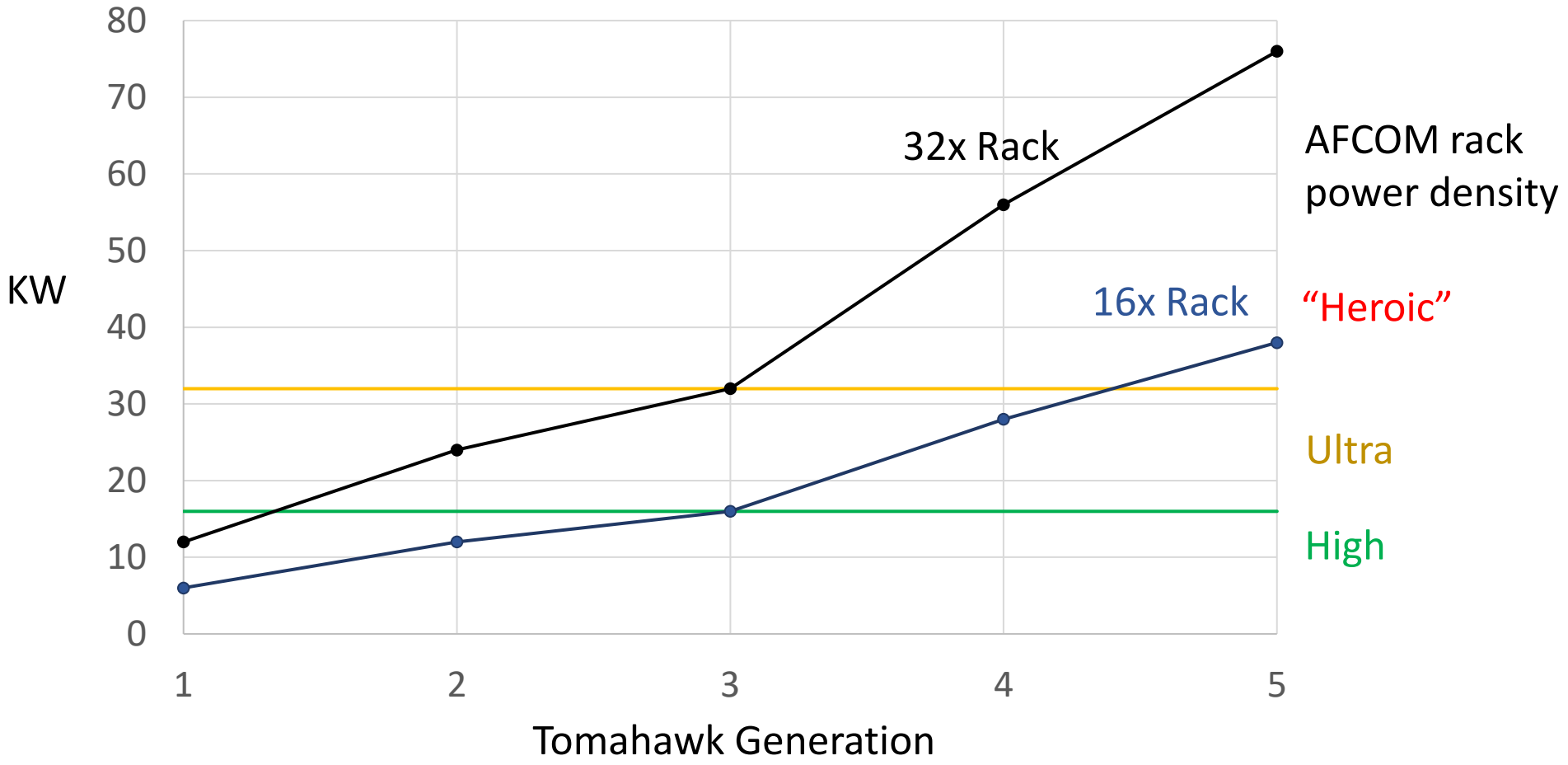
Tomahawk Switch ASIC				xSFP Optics	
Gen.	BW	CMOS node	Design Ref Pwr.	BW	Design Ref Pwr.
	Tb/s	nm	W	Gb/s	W
1	3.2	28	165	100	3
2	6.4	16	300	200	6
3	12.8	16	390	400	10
4	25.6	7	540	800	18
5	51.2	5	700	1600	28

Component, Line Card & Rack Power

Tomahawk Switch ASIC				xSFP Optics		HLC		Rack	
Gen.	BW	CMOS node	Design Ref Pwr.	BW	Design Ref Pwr.	32x	Total	32x	16x
	Tb/s	nm	W	Gb/s	W	W	W	KW	KW
1	3.2	28	165	100	3	100	360	12	6
2	6.4	16	300	200	6	200	750	24	12
3	12.8	16	390	400	10	320	1000	32	16
4	25.6	7	540	800	18	580	1750	56	28
5	51.2	5	700	1600	28	900	2400	76	38

AFCOM rack power density: Low ≤ 4KW < Medium ≤ 8KW < High ≤ 16KW < Ultra ≤ 32KW < "Heroic"

Air Cooled Rack Card Density is Limited by Power Dissipation



Vertical Line Card (VLC)

Thank you