A Single-Chip 5-V 2400-b/s Modem

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Abstract—**A single-chip split-band 2400-b/s modem has been implemented in a 3-μm CMOS process. A high level of integration results in a low-cost, high-performance modem. Single-ended analog switched-capacitor circuitry and an application-specific digital signal processor (DSP) combine to perform all modem signal processing. The transmit processing is performed almost entirely in the analog domain. The receiver is composed of a DSP and an analog front end (AFE). The IC also supports a number of lower speed (≤ 1200 b/s) split-band modem standards. The chip occupies 68.8 mm² and dissipates 120 mW while operating off a single 5-V supply. System and circuit aspects of the design will be discussed, and the measured performance of the IC will be summarized.**

I. Introduction

VOICE-BAND modems provide an efficient means of sending data over the public switched telephone network. Such modems can transmit and receive on an "as-needed" basis, thereby keeping costs low. V.22bis is a split-band, full-duplex, 2400-b/s modem standard for data transmission over two-wire phone lines [1]. An IC which meets all the V.22bis specifications has been implemented in a 3-μm CMOS technology. The IC makes extensive use of analog switched-capacitor circuits. An application-specific digital signal processor (DSP), which employs a reduced instruction set (RISC) architecture, is incorporated on the same substrate. The DSP handles the "back-end" processing in the modem receiver. The main goals of the IC design were to meet the V.22bis requirements, to minimize total die area and power dissipation, and to provide backward compatibility for many of the popular, lower speed modem standards. Given the system requirements, a great deal of flexibility and functionality had to be incorporated into the analog circuitry as well as in the DSP.

Some key features of the modem IC can be summarized as follows: 1) it performs all transmit signal processing and the front end of the receiver in the analog domain; 2) the DSP implements the "back-end" processing in the receiver (i.e., adaptive equalization, gain control computations, timing recovery calculations, carrier recovery, and decisions); 3) all analog circuits are single ended rather than fully differential to save IC area; 4) it includes everything except an off-chip hybrid; and 5) in addition to 2400 b/s, it can operate at 1200-, 600-, and 300-b/s data transmission rates.

This paper discusses the IC design, both at the circuit and system level. As background, the V.22bis specifications and the specifications of the optional slower speed modes are briefly summarized. Partitioning of the modem functions between analog and digital is discussed. Focusing on the 2400-b/s mode, the IC is explained in detail, first on the transmit side and then the receive side. Finally, measured performance of the IC functioning as a V.22bis modem is presented.

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II. Modem System Requirements

A. V.22bis Requirements

V.22bis is an internationally accepted modem standard for split-band, full-duplex, 2400-b/s transmission of data over the public switched telephone network [1]. (A V.22bis modem is often referred to as a 224 modem in the United States.) A brief summary of the V.22bis recommendations follows.

a) The modem is full duplex, transmitting in two nonoverlapping frequency bands. The high band is centered at 2400 Hz; the low band is centered at 1200 Hz. Each band occupies roughly 600 Hz of bandwidth. The baud rate is 600 Hz, with 4 b being transmitted each baud.

b) The modulation scheme is quadrature amplitude modulation (QAM) with a 16-point signal constellation. The baseband shaping is raised cosine with 75% excess bandwidth.

c) The dialing modem is designated the "originating" modem and transmits in the low band with a 1200-Hz carrier. The "answering" modem transmits in the high band with a 2400-Hz carrier. Upon answering, an answer tone is sent to initiate the handshake.

d) The receiver must have an adaptive equalizer. (This is recommended due to the closeness of signal constella-

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TABLE I
COMPARISON OF MODEM STANDARDS

modem standard	bit rate (bps)	modulation type	low band (Hz)	high band (Hz)	answer tone (Hz)
V.22bis/224	2400	QAM	900-1500	2100-2700	2100/2225
V.22/212A	1200	DPSK	900-1500	2100-2700	2100/2225
V.22 fallback	600	DPSK	900-1500	2100-2700	2100
103	≤300	FSK	1020-1320	1975-2275	2225
V.21	≤300	FSK	930-1230	1600-1900	2100

tion points and the deleterious effect of intersymbol interference caused by nonideal transmission channels.)

e) Optionally, a guard tone may be added to the high-band transmitted signal.

f) The receiver dynamic range should be 40 dB.

g) Operation at 1200 b/s (compatible with the V.22 recommendation at that speed) is part of the V.22bis specification. Only four of the 16 signal constellation points are used in the 1200-b/s mode; this subset reduces the modulation to differential phase-shift keying (DPSK).

B. Lower Speed Modem Compatibility

A desirable feature of any new commercial modem is to maintain compatibility with existing lower speed modems. The V.22bis standard provides a mode for operating at 1200 b/s, compatible with V.22 modems at that speed. But many other modem standards are in widespread use. We chose to implement some of the popular lower speed modem standards: V.22, Bell 212A, Bell 103, and V.21 [1], [2]. A brief listing of pertinent specifications for these modems is given in Table I. Note that the V.21 and Bell 103 low-speed modems employ frequency shift keying (FSK), which is quite different than the DPSK/QAM modulation schemes.

III. SYSTEM-LEVEL PARTITIONING OF FUNCTIONS

The signal on the phone line is analog; the incoming and outgoing data are digital. The break between analog and digital circuitry in both the transmit and receive paths must be determined optimally considering the entire system goals and requirements. The adaptive equalizer requirement and the multimode operation (e.g., QAM, DPSK, FSK) suggested a digital implementation of the back end of the receiver.

A block diagram of the complete modem IC is shown in Fig. 1. A brief discussion of the block diagram follows; a much more detailed discussion is given in the sections below. The partitioning of the analog and digital processing is indicated by the dashed line. Almost the entire transmit channel is analog, including the modulators (QAM, DPSK, and FSK), bandpass filters, attenuator, and tone generator (for DTMF, answer, and guard tones). On the receive side, processing of the passband signal is handled in the analog domain. After amplification by the AGC and delay equalization, the signal is demodulated to baseband prior to analog-to-digital conversion. The DSP then handles the remaining receive signal processing.

In most applications, the modem IC is controlled by an external microprocessor which sets up the mode of operation and monitors the modem status over the 8-b microprocessor interface.

A. Analog / Digital Partitioning Comparisons

The analog/digital partitioning chosen in the IC will now be compared with alternative partitionings. Fig. 2 shows the modem with three different analog/digital partitionings indicated by the dashed lines labeled *A*, *B*, and *C*. For each of these partitionings, the requirements for data conversion, DSP multiplication rate, and equivalent analog multiplication rate are compared in Table II. The analog computational load is based on the clock rates employed in the modem IC as described below (see Figs. 3 and 5), where a multiply is counted wherever a multiplication would be required in an equivalent digital implementation. Note that the DSP load increases significantly (to just beyond the delay equalizers) when the DSP interface is moved from *A* to *B*. The DSP load increases by a factor of 20 because the sampling rates in the equalizers and low-pass filters are much higher than the baud-rate processing in the DSP in case *A*.

A number of two-chip modems that combine an analog front end and a general-purpose digital processor have been designed [3]–[6]. These modems typically use the partitioning at point *B* due to the processing power of the digital processors. The third partitioning, *C*, corresponds to a fully digital approach. Here the DSP loading is computed assuming all digital processing occurs at the minimum possible sampling rate (e.g., the bandpass filters (BPF's) operate at a 9600-Hz sampling rate). This approach has both a very high digital processing load and also requires a wider data bus to accommodate the larger ADC and DAC words, which are necessary to provide sufficient resolution and linearity in the absence of the analog BPF's. Given an analog/digital compatible CMOS process, *A* is the preferred partitioning.

B. Circuit Requirements Given the Selected Partitioning

A high-performance modem receiver can achieve a 10^{-5} bit-error rate with a SNR that is only a few decibels worse than theoretically predicted [7]. For V.22bis, an ideal receiver can achieve a 10^{-5} bit-error rate with a 14-dB input signal-to-noise ratio [8]. To assure the near-theoretical performance, it is important to keep all signal degradations to a minimum as the signal passes from the receive input pin of the IC to the output of the analog-to-digital converter. The receive BPF must adequately reject the large transhybrid signal while adding a negligible amount of noise to the weak received signal. Crosstalk from the transmitter and from the DSP into the receive signal path must be kept low. Considering only the noise added by the circuitry in the receive channel, a 25-dB SNR at the ADC output was the target. This gives an 11-dB margin over the theoretical value of 14 dB. Achiev-

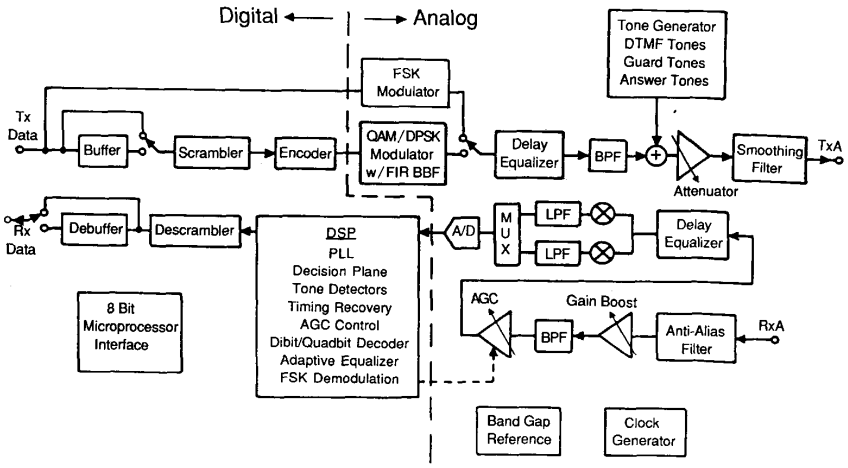

Fig. 1. V.22bis modem IC block diagram, showing the analog/digital partitioning.

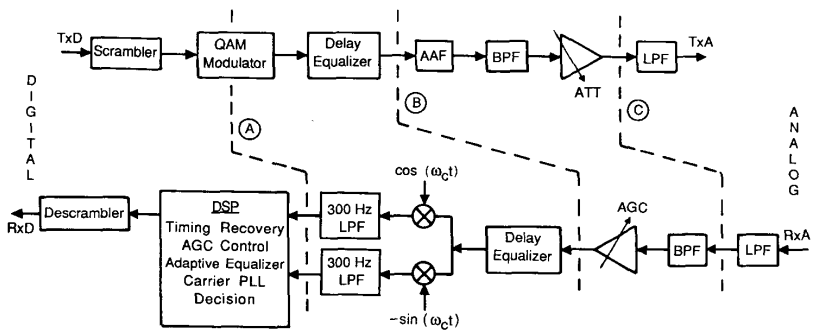

Fig. 2. Three different analog/digital partitionings.

TABLE II
COMPARISON OF THE THREE ANALOG/DIGITAL PARTITIONINGS SHOWN IN FIG. 2

Break at	Data Conversion	DSP Load	Analog Load
A	2 8-bit A/D at 2400 Hz 2 2-bit D/A at 9600 Hz	84 k mult/sec with 8-bit data	25 M mult/sec
B	1 8-bit A/D at 9600 Hz 1 8-bit D/A at 9600 Hz	1.7 M mult/sec with 8-bit data	23 M mult/sec
C	1 14-bit A/D at 9600 Hz 1 12-bit D/A at 9600 Hz	2.8 M mult/sec with 14-bit data	7.3 M mult/sec

ing this 25-dB SNR over the 40-dB receive input range was challenging given the 5-V power supply constraint. Careful scaling of the analog signal and a low noise floor at the output of the receive BPF were important design considerations.

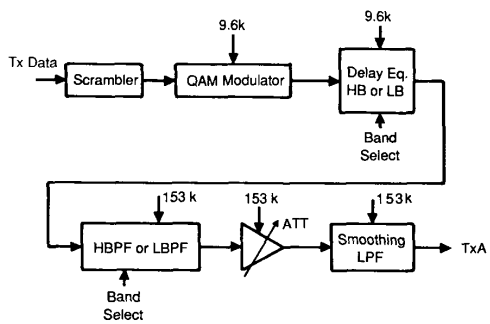

Fig. 3. Transmit signal processing. SC clock frequencies are shown.

IV. TRANSMIT SIGNAL PROCESSING

A block diagram of the transmit processing on the IC is shown in Fig. 3. In this mode, all clocks in the transmitter are derived from the master analog 921.6-kHz clock. The data are scrambled, and then a switched-capacitor (SC) quadrature amplitude modulator [3], [9] shapes the data with an SC baseband filter (BBF) and modulates by a carrier frequency of 1200 or 2400 Hz. The output of the modulator is further shaped in the passband by the transmit BPF and delay equalizer, which provide compromise magnitude and phase equalization for the typical phone line. The BBF and BPF combine to provide the required root 75% cosine spectral shaping of the transmitted signal.

The output of the BPF can be summed with a 550- or 1800-Hz guard tone signal produced by an on-chip tone generator [3] (Fig. 1). An SC programmable attenuator

sets the transmit power level to any value from −6 to −21 dBm in 1-dB increments. An output smoothing filter completes the transmit path.

V. The Bandpass Filters

There are two bandpass filters on the IC, one for the high band and one for the low band. At any time, one filter is connected in the transmit path and the other in the receive path as determined by the transmit frequency band selected. The major task of the receive BPF is to eliminate the large transmitted signal which overwhelms the weak received signal in the worst case (i.e., −6-dBm transmit level, −43-dBm receive level, minimal transhybrid loss) while maintaining adequate SNR at its output. The major task of the transmit BPF is to provide the requisite transmit spectral shaping while keeping distortion low (note that second harmonic distortion of the low band falls in the high band). The BPF's had to meet some stringent specifications: provide a minimum of 25-dB SNR at the receive BPF output under worst-case conditions and maintain the tight magnitude and group delay tolerances required by the V.22bis specification (±0.75 dB within ±200 Hz of the center frequency, ±150 μs within ±300 Hz of the center frequency). In addition, the low-band filter must maintain less than −60-dB second harmonic distortion and provide greater than 45 dB of guard tone attenuation.

A key to the filter design was optimization of dynamic range. Extensive simulation of pole–zero combinations and biquadratic section ordering were required to minimize filter noise [10].

The BPF's were realized as cascaded biquads. The low-band filter has a center frequency of 1200- and 900-Hz bandwidth. A 14th-order magnitude section is coupled with a sixth-order delay equalizer. The high-band filter has a center frequency of 2400- and 900-Hz bandwidth. It is a 12th-order magnitude section, and the corresponding delay equalizer is fourth order. A 153.6-kHz sampling rate was chosen for the magnitude sections of the filters. This high clock rate reduced noise folding and eased the antialias requirements. The delay equalizers are clocked at 9600 Hz. This low clock rate was chosen to reduce IC area by reducing capacitor ratios and to ease the settling time requirement of the op amps. Wide-band noise is aliased in-band due to the low sampling rate, but this noise is not a concern in the transmitter. In the receiver, the effect of the noise is greatly reduced by placing the delay equalizer after the AGC gain stage (Fig. 1). Due to the low sampling rate, the delay equalizers were designed directly in the z domain using the equations given in [11] and a special optimization program.

Fig. 4 shows the measured characteristics of the BPF's. The slight peaking at the high end of the high BPF compensates for the roll-off in the typical phone line. Note the excellent rejection (> 65 dB) of the adjacent band, which is required for receive-side processing, and the deep notches at the guard tone frequencies of 550 and 1800 Hz in the low-band filter.

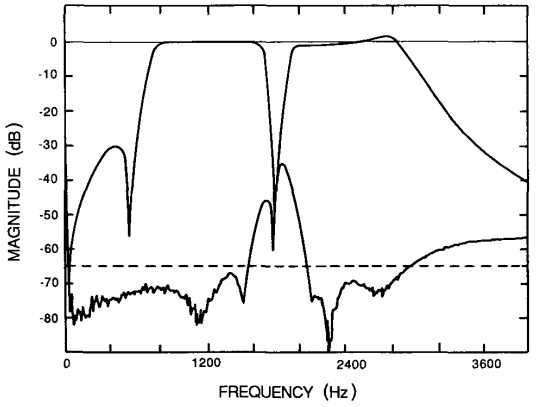

Fig. 4. BPF magnitude responses.

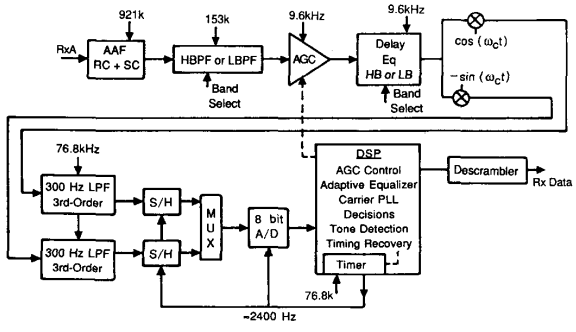

Fig. 5. Receive signal processing in the IC. SC clock frequencies are shown.

VI. Receive Signal Processing

The receive-side signal processing on the IC is shown in Fig. 5. The receiver employs an analog front end (AFE), which includes all circuitry up to and including the ADC, and a DSP. The received signal first passes through *RC* and SC 4-kHz low-pass biquad filters for antialiasing prior to being sampled by the receive BPF. The BPF eliminates the local transmitted signal. After band-limiting, the signal is immediately downsampled at a 9600-Hz rate by the SC gain stage. This programmable SC gain stage, controlled by the receive DSP, amplifies the received signal. After amplification, the signal passes through the delay equalizer clocked at 9600 Hz. The passband signal is then mixed to baseband by fixed-frequency quadrature carriers: $\cos(\omega_c t)$ and $-\sin(\omega_c t)$ with $\omega_c = 2\pi(1200\text{ Hz})$ or $2\pi(2400\text{ Hz})$. The demodulation produces double-frequency components which are eliminated by the two 300-Hz low-pass filters (LPF's) following the multipliers. On command from the timing recovery algorithm, which is implemented in the DSP, the two sample-and-holds (S/H's) simultaneously sample the in-phase and quadra-

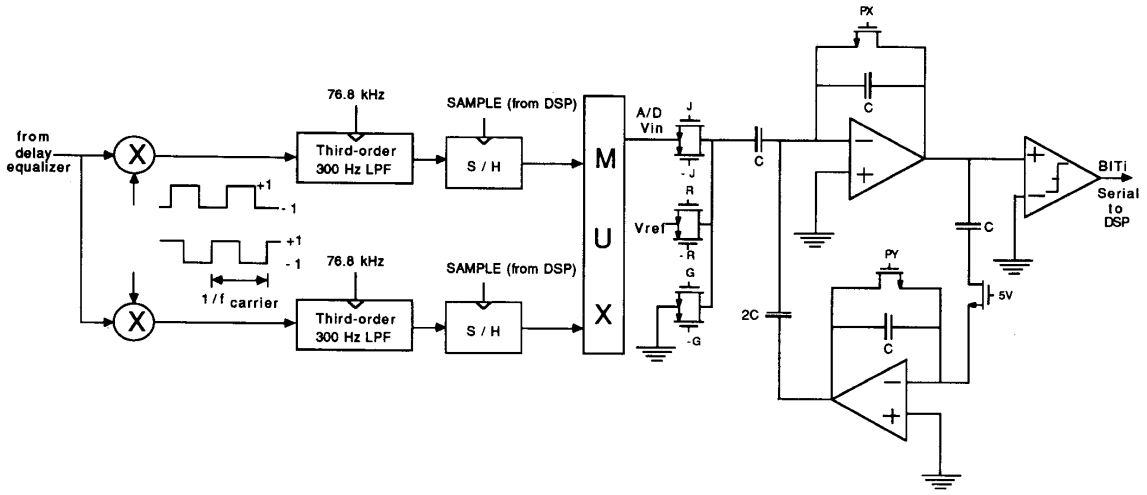

Fig. 6. Details of the fixed-frequency demodulator and 8-b ADC.

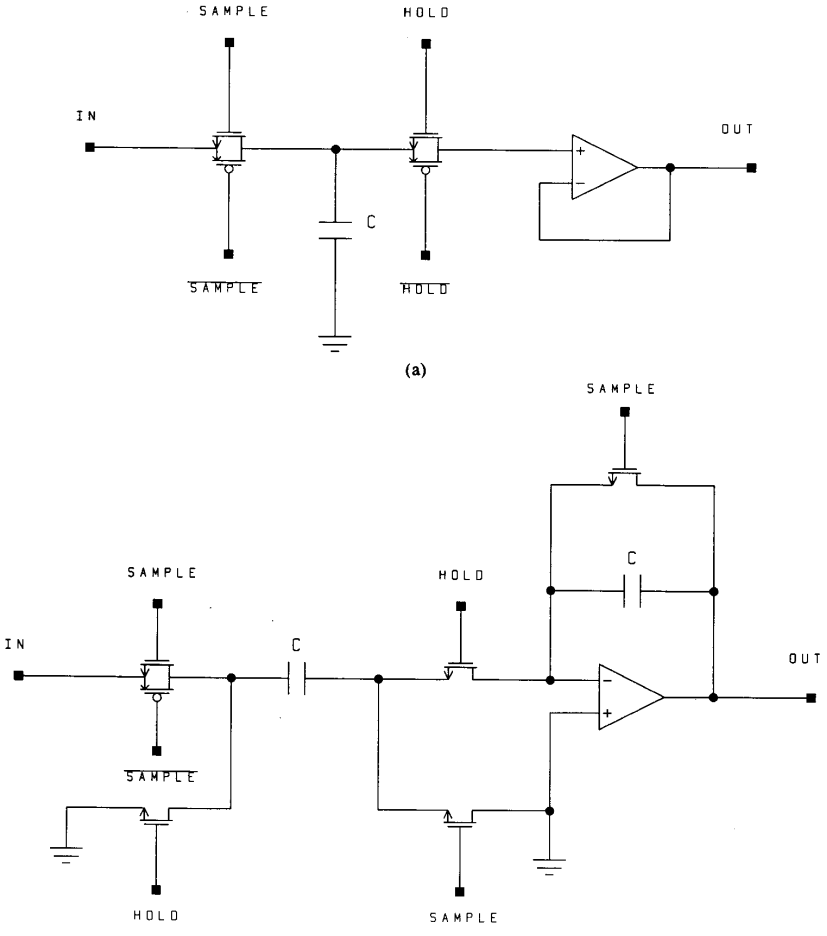

Fig. 7. (a) Conventional S/H requiring an op amp with large input common-mode range. (b) S/H with no input common-mode swing required of the op amp.

ture signals. The samples are then converted to two's complement, 8-b digital values by a time-multiplexed cyclic analog-to-digital converter [12]. The two conversions occur at a 2400-Hz rate, the sampling clock being four times the recovered 600-Hz baud-rate clock. These digitized sample values are passed serially to the DSP. The DSP performs the remaining receive signal processing.

A. Fixed-Frequency Demodulation

An on-chip timer under DSP control counts down a crystal-derived 76.8-kHz clock to four times the recovered 600-Hz baud rate clock (Fig. 1). The two 300-Hz LPF's preceding the S/H's are operated off the same 76.8-kHz clock which drives the receive timer. This 2400-Hz clock is the sampling clock for the two S/H's. Since this recovered clock is not synchronized to the crystal-derived 76.8-kHz clock that drives the LPF's, aliasing is a concern. The combination of the SCFs' low-pass response and the high-frequency attenuation due to $\sin(x)/x$ proved adequate from an antialias standpoint.

The highly oversampled 300-Hz LPF's allow simple square waves in phase quadrature to be used for the demodulation process, replacing the $\cos(\omega_c t)$ and $-\sin(\omega_c t)$ multiplications shown in Fig. 5. This is shown in Fig. 6. The high-frequency demodulation products caused by the square-wave demodulation are sufficiently attenuated by the 300-Hz LPF's. To avoid the common-mode swing limitations imposed by an op amp operating from a 5-V supply, a noninverting SC gain stage, shown in Fig. 7(b), was used as the S/H rather than the conventional S/H, shown in Fig. 7(a).

B. Gain Stage

A programmable SC gain stage amplifies the received signal. The gain range is 0 to 48 dB in 0.375-dB steps. The receive gain amplifier requires low effective input offset voltage to avoid large dc output offset which can cause clipping at the maximum gain setting. First-order autozeroed high-pass filters (HPF's) are placed before and after the gain stage to block dc offset, as is shown in Fig. 8(a). The first half of the gain stage (i.e., the input HPF and first gain stage) is shown in Fig. 8(b). The z-domain transfer function of the HPF is

$$H(z) = \frac{C_1}{C_{FB}+C_R}\,\frac{1-z^{-1}}{1-\dfrac{C_{FB}}{C_{FB}+C_R}z^{-1}}. \qquad (1)$$

The 9600-Hz sampling rate in the gain stage greatly relaxed settling requirements and reduced capacitor ratios in the HPF's.

Monotonicity of the gain as a function of the digital gain control word is essential to assure proper operation of the gain control loop. The 48-dB gain was implemented in two stages. The first employed a binary-weighted capacitor array to give accurately defined gain values in 6-dB steps. A second cascaded gain stage provided the 0.375-, 0.75-, 1.5-, and 3.0-dB steps. Large capacitors assured accurate ratios and therefore a monotonic gain characteristic.

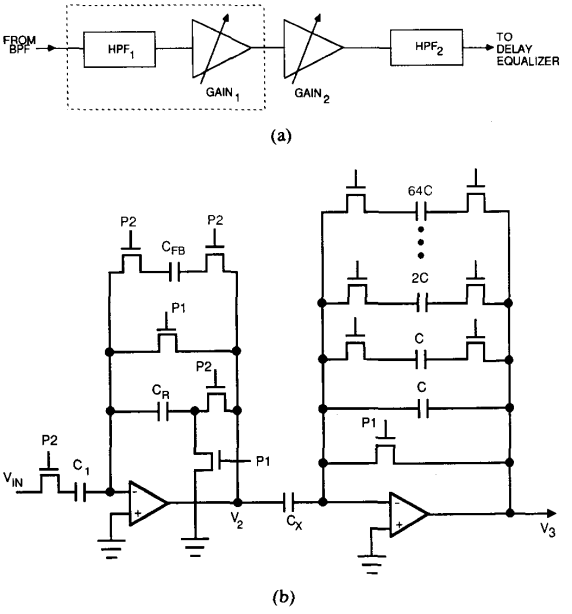

Fig. 8. (a) Programmable gain stage with HPF's. (b) Schematic of first half of programmable gain stage: input HPF and first gain amplifier.

TABLE III
DSP COMPUTATIONAL LOADING

	Number of Moves	Multiplies
Adaptive equalizer output	440	44
Equalizer coefficient update	620	44
AGC control loop	150	2
Timing Recovery	38	0
Phase-locked loop	50	9
Special functions	80	8
Interrupts	130	0
Decision plane	70	0
General mode control	240	8
Total	1818	115

C. Digital Signal Processor

Included on the receive side is an application-specific RISC DSP that handles the complex receiver algorithms [13]: adaptive equalization, AGC control, timing recovery, carrier recovery phase-locked loop, signal constellation decisions, and detection of signaling tones. Prior to electrical design, the DSP architecture and instruction set were simulated against the major modem algorithms. These simulations in conjunction with the AFE design indicated that a processor with an 8-b word size and 16-b coefficients would produce a modem with acceptable performance. Parameters for the algorithms were derived from channel simulations, indicating a computational load of roughly 2000 instructions per baud (see Table III). Circuit simulations in a 3-μm CMOS process confirmed

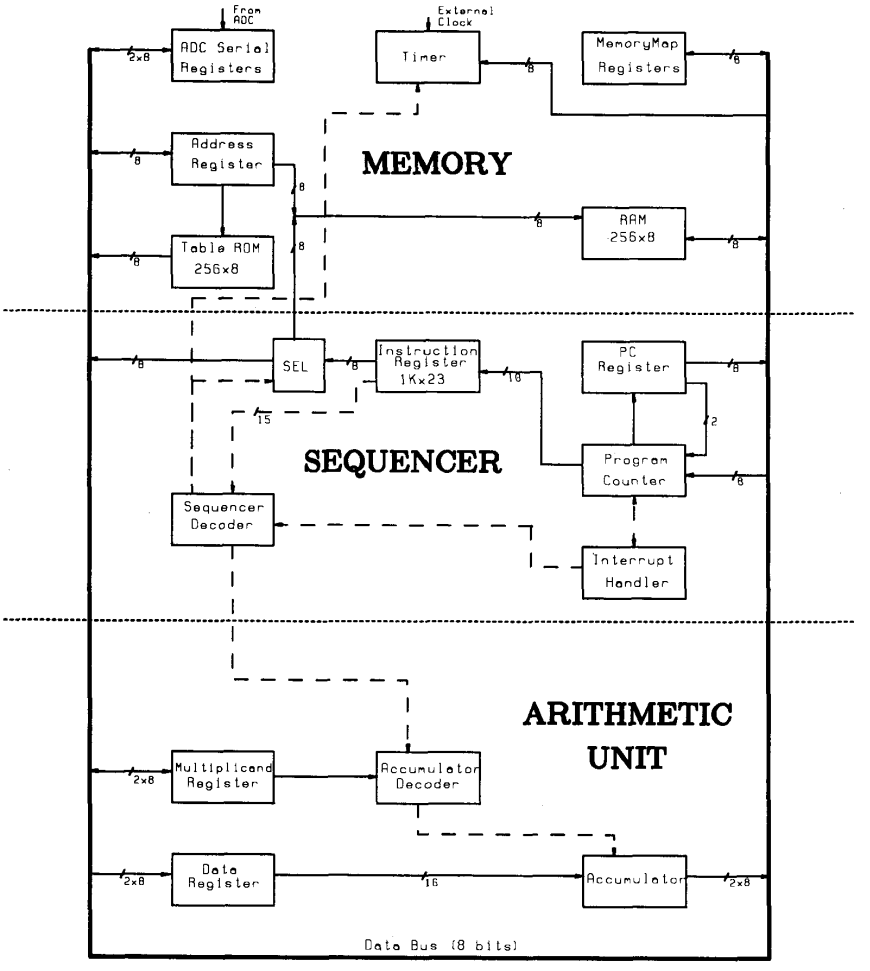

Fig. 9. DSP block diagram.

that the architecture could be designed with a 5.5-MHz instruction clock, thus verifying the sufficiency of the DSP which has as its goals: minimization of complexity, noise generation, power dissipation, and size. The 5.5-MHz instruction clock permitted the 90-mW power budget for the DSP to be maintained.

A RISC architecture was used for its simplistic decode requirements. Architectural features of the DSP are shown in Fig. 9. In the figure, the dashed lines are control signals. Included are instruction ROM (1024×23), data RAM (256×8), table ROM (256×8), a timer, an address register, single-level hardware program counter storage (to allow for interrupts), an arithmetic unit (AU), and special hardware interface to the analog blocks and the microprocessor port. A 10-b program counter is required to address the instruction ROM, which creates a size conflict with the chosen 8-b bus size. To reduce hardware requirements, we implemented the CALL mechanism by paging (using four pages). One level of hardware stack is used to allow interrupts, with the balance of the stack having the eight LSB's of the program counter stored to RAM. A second, smaller ROM (256×8) is used for table look-up which stores filter coefficients and values of $\sin(\theta)$.

The DSP operates at a 180-ns cycle time; the receiver algorithm repeats at the 600-Hz baud rate. As a result, there are 9216 instruction cycles available every baud time. Noting the large number of machine cycles available, the simple shift-and-add algorithm is used for all multiplies. A subroutine was created for multiply with the result that an 8×8 multiply consumes ten clock cycles. The left and right shifts, implemented by the AU's data and multiplicand registers, respectively, are used for signal scaling. Scaling allows maximum precision to be maintained as the various algorithms are applied to the incoming signal values. The bit-oriented functions—set, clear, and branch-on-condition—are implemented using the arithmetic functions. Also, with over 9000 instructions per baud, there is enough time for implementation of complex high-performance receiver algorithms.

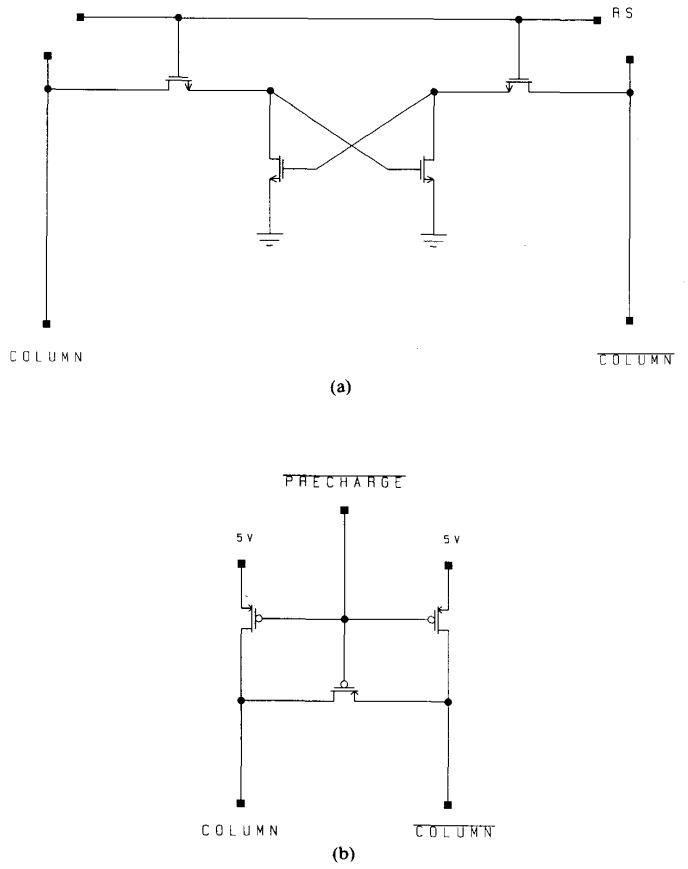

Fig. 10. Dynamic RAM: (a) four-transistor cell, and (b) column precharge. (*Continued.*)

A locally refreshed RAM was chosen for the DSP. A four-transistor dynamic RAM cell (Fig. 10(a) was selected because its refresh strategy works well with the captive nature of the design. The RAM is arranged into 256 8-b words which are physically realized by 64 columns and 32 rows. To reduce power and minimize access time, precharging is utilized in both the address decoder and column refresh circuitry (Fig. 10(b), (c)). During the refresh time, all *RS* lines are discharged, the address lines are set to their final value, the address decoder internal nodes are precharged, and the column and $\overline{\text{column}}$ lines are precharged. At the transition out of the precharge mode, one row is selected. Each row contains eight words with the input and output data from the bus being steered to the desired word. The unselected bits in the row are refreshed along with the bits of the selected word when *RS* is high. To ensure refreshing of all bits in the RAM, the DSP firmware incorporates a short loop that accesses one word in each RAM row every baud period. Reading and writing of the RAM are performed by the circuitry shown in Fig. 10(d). Because of the level of the signals in the RAM, a ratioed inverter is sufficient for use as a sense amplifier.

The basic control of the DSP is divided between external control from the microprocessor port and internal control via various calculated quantities based on the current demodulation mode. It is this distributed control that allows the external microprocessor to choose the macro state transitions implemented in the DSP and allows the DSP to produce quick responses to certain micro functions.

VII. Other Circuit Blocks

A detailed block diagram of the IC was shown in Fig. 1. A few of the functional blocks have not been discussed so far. A bandgap reference voltage is generated on-chip using the substrate n-p-n transistor in the p-well CMOS process. This is the reference for the ADC, modulator, and tone generator.

An on-chip crystal oscillator was designed for operation at 11.0592 MHz. This frequency is integer related to the

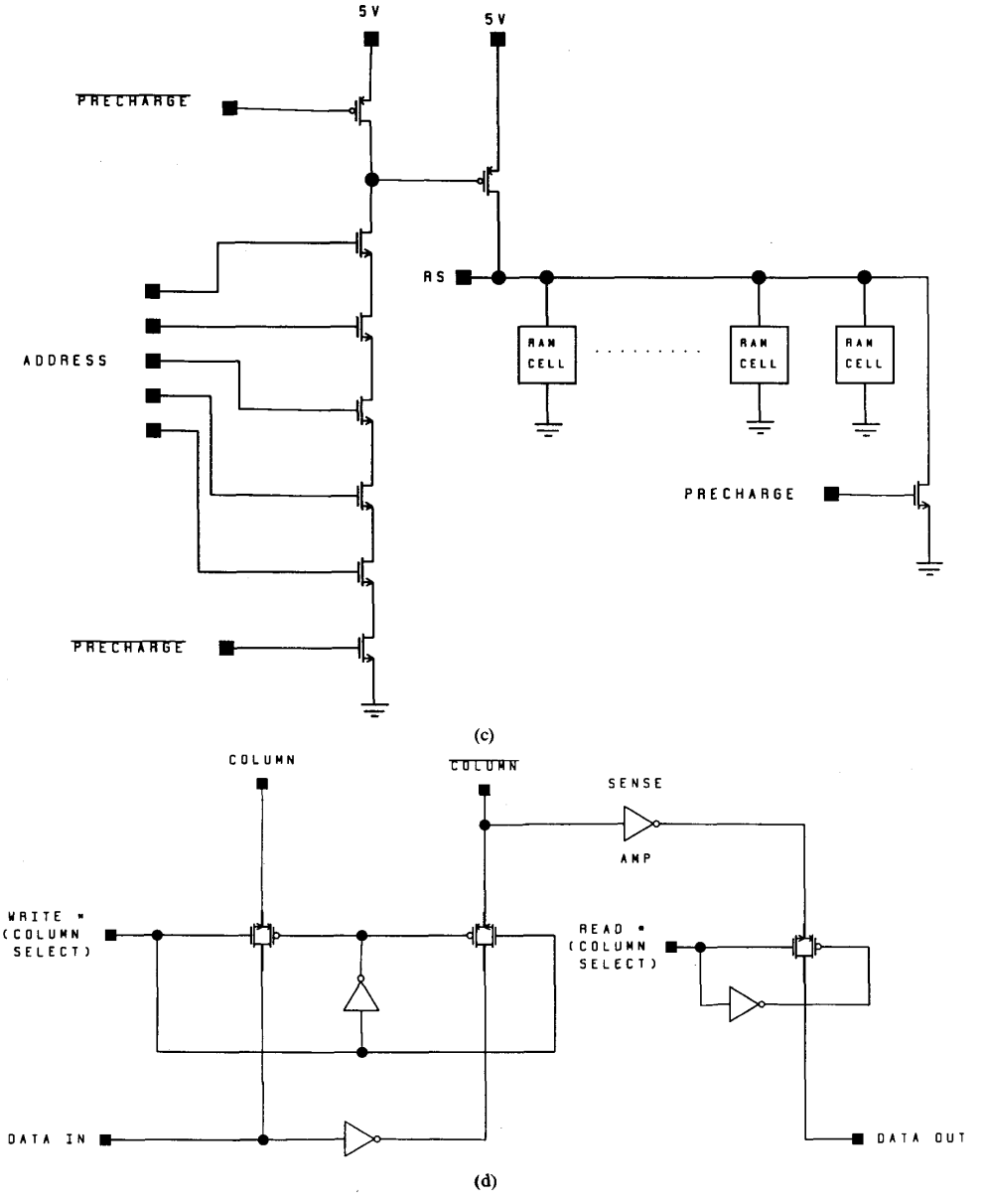

Fig. 10. (*Continued.*) Dynamic RAM: (c) address decoder with precharge, and (d) I/O circuitry.

bit-rate clocks and is high enough to drive candidate control microprocessors. The output of the crystal oscillator is divided down to give the clocks required by the various circuit blocks.

Three basic op amps were used repeatedly on the chip. Sufficient signal swing for operation at low supply (4.5 V) required careful signal scaling and also constrained the op-amp selection. A two-stage internally compensated op amp providing an open-loop gain of 10000, a 1-MHz unity-gain bandwidth, and an output voltage swing to within 0.25 V of the supplies was used extensively. For driving off-chip loads as low as 10 kΩ in parallel with 100 pF, an op amp with an n-p-n output stage was used.

Where faster settling was required (e.g., in the SCF's clocked at 921 kHz), a folded-cascode op amp (Fig. 11) with somewhat reduced output voltage swing was employed. By using large W/L ratios for the p-channel transistors $M3$–$M6$, the positive output swing was able to reach within 0.5 V of the supply. The output capacitive loading presented naturally by the SC circuits served as

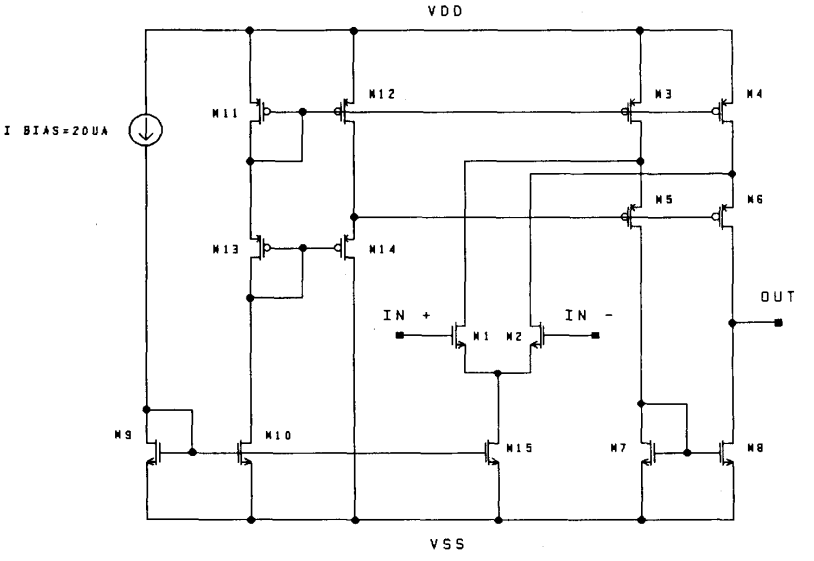

Fig. 11. Folded-cascode op amp.

the compensation capacitor. With a 10-pF load, the unity-gain bandwidth is 10 MHz; the dc gain is 1000.

VIII. Minimizing Digital-to-Analog Crosstalk

As mentioned above, all analog SC circuits on the modem IC are single ended. As such, coupling of noise generated by the DSP into the analog circuits was a major concern. A number of precautionary steps were taken to minimize this crosstalk.

The analog and digital circuits were physically separated as much as possible, with substrate tie-downs connected to clean analog supplies surrounding the analog circuitry. Separate power supply metal lines were run for the analog and digital circuitry, and for the receive and transmit circuitry. These metal lines meet at the power and ground pads. All sensitive analog signal nodes were shielded from the substrate by wells which are tied to a clean analog supply. All clocks in the analog circuits are derived by integer division from the master analog 921.6-kHz clock, which itself is generated by a divide by six from the DSP's 5.5-MHz clock. By delaying the 921.6-kHz clock edge from the 5.5-MHz clock edge, it is assured that all SC circuits sample when the DSP is not switching. By using a single 5-V power supply, the digital noise generation was minimized.

IX. Multimode Testing

Test access in this mixed analog/digital VLSI design addresses several different areas: device verification, system performance, and user diagnostics. This design has several loopback modes (e.g., transmitter analog output looped into the receiver analog input) which, when properly set up, allow the transmit and receive functions to be exercised as in an actual system configuration. The chip also has a test mode that allows various functions, such as filters, the gain stage, and the ADC to be checked individually. These tests allow for fault isolation and may give an indication of poor modem performance. A third test function is performed each time the DSP is brought out of the reset state. This is a self-test which checks for RAM and constant ROM failures and utilizes many of the DSP control and data paths, thus achieving good fault coverage. The resultant check sum is provided to the control microprocessor via the register interface.

The final test mode provides the real-time output of the DSP state. This information can be used to display many system quantities (e.g., the receiver's signal constellation) that are useful in modem firmware development. To enable this mode, several control signals change the IC from a standard device on the microprocessor bus to a controller that dumps the real-time program counter and corresponding data word. This set of test modes, both

TABLE IV
Measured Performance of the IC

Technology	3 μm CMOS: double poly, single metal
Power Supply	5 V ± 10%
Power Dissipation	120 mW
Die Size	68.8 mm^2
Number of transistors	60,000
Number of op amps	61
DSP cycle time	180 nsec
DSP computational loading	55 % in 2400 bps mode
Modes supported	CCITT V.22bis, V.22, V.21 Bell 212 and 103
ADC	8 bits ± 0.5 LSB
Receiver dynamic range	-3 dBm0 to -44 dBm0
SNR for 10^{-5} bit-error rate	17 dB at 2400 bps over receiver dynamic range

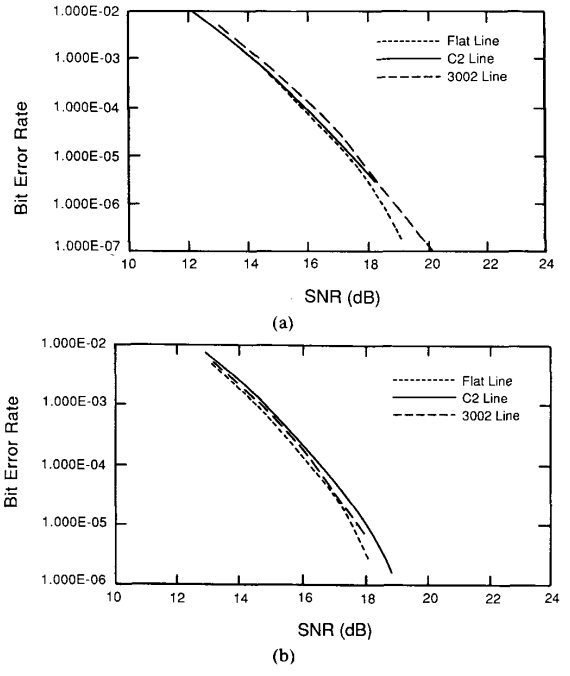

Fig. 12. 2400-b/s modem performance: bit-error rate versus input SNR. (a) Low band. (b) High band.

analog and digital, is implemented with a die size penalty of a few percent.

X. Measured Performance

The IC was tested to determine how well each functional block was performing and how well it functions as a V.22bis modem. Table IV summarizes the measured data. The receiver's bit-error-rate curves for the 2400-b/s mode are plotted in Fig. 12. Plots for four different phone lines are shown. A 10^{-5} bit-error rate is achieved with less than 18-dB signal-to-noise ratio (the noise is C-message weighted). This performance is maintained over a 40-dB input range. These results demonstrate that the IC performs very well as a V.22bis modem.

A photograph of the IC is shown in Fig. 13. The analog circuitry covers roughly 40% of the active area.

XI. Conclusion

A system-specific IC which combines single-ended analog, switched-capacitor circuitry, and a custom DSP has been successfully designed for the V.22bis modem application. The IC was designed to optimize the overall system cost and performance. Minimum sampling rates have been used in the DSP and in the switched-capacitor circuitry to minimize area and power dissipation. In addition to V.22bis, a number of lower speed modems have also been implemented. Measured modem performance meets or exceeds all V.22bis requirements.

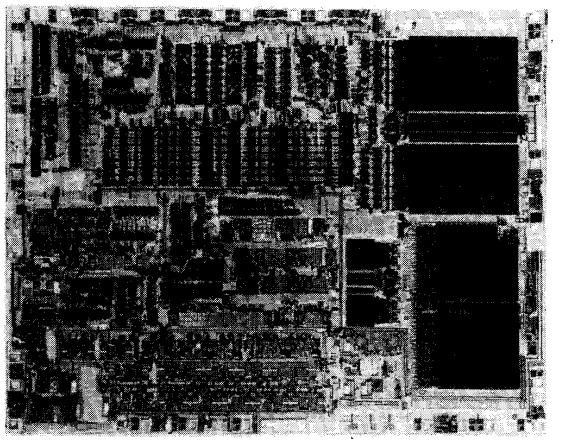

Fig. 13. Die photograph of the modem IC.

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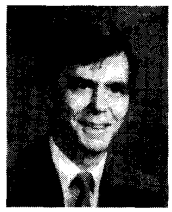

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