Photonic Integration for High-Volume, Low-Cost Applications

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ABSTRACT

To date, photonic integration has seen only limited use in a few optical interface applications. The recently adopted IEEE draft standards for 40 Gb/s and 100 Gb/s Ethernet single-mode fiber local area network applications will change this situation. Although first generation implementations will use discrete components based on existing technologies, long-term requirements for significant reduction in cost, size, and power of 40 Gb/s and 100 Gb/s transceivers will lead to a broad demand for photonic integration. Both hybrid planar lightguide circuit and monolithic photonic integrated circuit are feasible approaches that meet the requirements of the new IEEE standards.

INTRODUCTION

Photonic integration is not used in the manufacture of most optical interfaces. This is despite the development of many different integration technologies and many examples of photonic integration in journal articles [1] and conference papers [2]. The principle reason is that optical interface architectures, defined in widely used standards, offer no opportunities for integration. For example, almost all IEEE-specified architectures for 100 Mb/s, 1 Gb/s, and 10 Gb/s optical interfaces require only a single directly modulated laser (DML). In such architectures, referred to as serial, there is nothing to optically integrate. Some longer-reach IEEE and International Telecommunication Union (ITU) standards, although still serial, use an electro-absorption modulated laser (EML). The EML integrates a single laser and modulator on a chip, representing the first wide use of photonic integration. A 10 Gb/s standard that could have benefited from photonic integration because it requires four DMLs (10GBASE-LX4) was supplanted by a serial standard (10GBASE-LRM), eliminating it as a potential market driver for photonic integration technology.

The IEEE recently adopted three draft standards for 40 Gb/s and 100 Gb/s single-mode fiber (SMF) optical interfaces: 40GBASE-LR4 and 100GBASE-LR4 for reaches up to 10 km, and 100GBASE-ER4 for reaches up to 40 km. Formal adoption is projected in 2010 [3]. These standards all require four lasers and wavelength division multiplexing (WDM) and represent significant long-term, high-volume, commercial opportunities for integrated photonic circuits. The candidate functions for photonic integration are:

- 40GE 10 km quad 10 Gb/s CWDM 1310 nm DML transmitter
- 100GE 10 km quad 25 Gb/s LAN WDM DML 1310 nm transmitter
- 100GE 10 km/40 km quad 25 Gb/s LAN WDM EML 1310 nm transmitter

First generation implementations of these functions will use discrete transmit components (four single un-cooled DMLs for 40GE and four single cooled EMLs for 100GE) with fiber connecting them to a discrete WDM multiplexer [3]. This is driven by time-to-market considerations. However, in the long term, demand for high-volume, low-cost, small size transceivers will lead to broad industry use of photonic integration technology because this is the only way to meet aggressive size and cost targets. The four discrete transmitters and discrete multiplexer will be replaced by a single integrated transmitter. Hybrid planar lightguide circuit (PLC) and monolithic InP photonic integrated-circuit (PIC) technologies are feasible today for use in integrated transmitter development.

SUCCESSFUL COMMERCIAL PHOTONIC INTEGRATION EXAMPLES

VERTICAL CAVITY SURFACE EMITTING LASER ARRAYS

The IEEE also recently adopted draft standards for parallel multi-mode fiber (MMF), multi-fiber push on (MPO) connector optical interfaces, 40GBASE-SR4 and 100GBASE-SR10, for reaches up to 100 m [3]. These exploit a mature optics integration technology: vertical cavity surface emitting laser (VCSEL) array, which has been shipping in high volume at lower channel data rates, for example, in SNAP12 transceivers. To support these new MMF standards, four or twelve 10 Gb/s VCSEL element linear arrays are fabricated using the same process as for a single VCSEL used in serial 10 Gb/s MMF transceivers like 10GBASE-SR, with additional optimization

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of top masks for alignment during assembly onto flex circuits. Because none of the VCSEL elements are optically connected in the arrays, they are not strictly photonic circuits. However, VCSEL arrays demonstrate one of the important characteristic of photonic circuits. The yield of VCSEL arrays is inversely logarithmic with the VCSEL channel number [3], leading to significantly lower cost for a parallel transceiver than the cost of the same number of channels implemented with discrete transceivers.

EML

The EML is the only broadly available, commercially successful component that can be classified as a photonic circuit. An EML integrates and optically interconnects two components: a distributed feedback (DFB) laser and an electroabsorption (EA) modulator on a monolithic InP chip [4]. EMLs are used in many optical interfaces, for example, IEEE 10GBASE-ER 10 Gb/s 40 km transceivers and ITU G.693 40 Gb/s 2 km transceivers. The modest level of integration of EMLs leads to high yields, enabling lower cost and size than alternatives using discrete components.

EML Arrays

An array of ten 10 Gb/s EMLs integrated with an arrayed waveguide grating (AWG) mux on a single InP chip has been reported [5]. The chip is used as a key enabling technology in high-end wide area network (WAN) systems and has been successfully used in the field for several years. The technology is proprietary, its cost structure has not been published, and the chips are not sold or bought commercially. Although demonstrating what is technically possible, this technology has not been a photonic integration driver for the optics industry, because no market has been created for these chips.

Tunable Lasers

Recently, tunable laser sources have had to use photonic integration technology to enable small form factor transceivers. Several types of tunable lasers, each consisting of multiple monolithic photonic sections along a waveguide were integrated with Mach Zehnder modulators to achieve high-speed modulation with a well-controlled chirp. Semiconductor optical amplifier (SOA) sections also were added to boost output power. An example of a multi-section tunable laser was reported in [6].

IEEE 40 Gb/s and 100 Gb/s SMF Draft Standards

40GBASE-LR4 Standard

Figure 1 shows a block diagram of transceiver architecture for the 40GBASE-LR4 (10 km) standard. The transmitter has four 10 Gb/s signal paths, supporting either a retimed or un-retimed electrical interface. The output of the four DFBs is combined optically in the mux for transmission over one SMF. Other than the optical multiplexer and demultiplexer, the architecture replicates four single 10 Gb/s channels, like those in the 10GBASE-LR standard. This was done to permit quick time-to-market development, using existing discrete 10 Gb/s components.

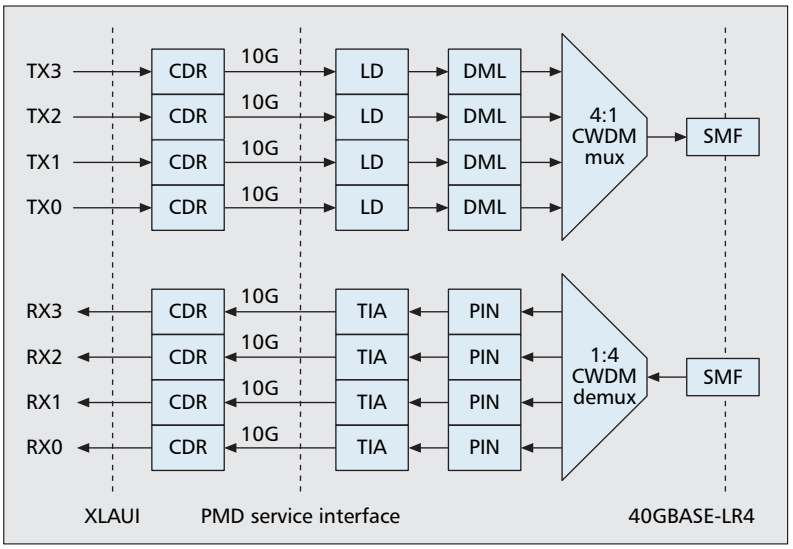


Figure 1. *40GBASE-LR4 transceiver architecture. XLAUI electrical interface requires CDRs; PMD service interface does not.*

The coarse-wavelength-division multiplexing (CWDM) optical wavelength assignments are shown in Table 1.

The 20 nm grid permits use of un-cooled DFBs, as the approximately 7 nm laser wavelength drift over the operating temperature range fits within the CWDM pass-band.

100GBASE-LR4 and 100GBASE-ER4 Standards

Figure 2 shows a block diagram of the transceiver architecture for the 100GBASE-LR4 (10 km) and 100GBASE-ER4 (40 km) standards. The four channel count was selected as leading to a reasonable component count in discrete and photonic integration implementations. The channel data rate of 25 Gb/s is relatively low risk because of the commercial availability of 40 Gb/s EMLs and ongoing research toward 25 Gb/s DMLs. The EML solution has the advantage of lower dispersion penalties due to the low chirp of the EA modulator and is the only feasible solution for ER4 (40 km reach). Future DML solutions may offer higher output power and lower electrical power dissipation, but will be usable only for LR4 (10 km reach). An electrical interface rate of 10 Gb/s per channel was selected as the best match to existing complementary metal-oxide semiconductor, application-specific integrated-circuit (CMOS ASIC) interface technology.

The local area network (LAN) WDM optical wavelength assignments are shown in Table 2.

The 800 GHz (~5 nm) channel spacing is an optimization between relaxed wavelength accuracy requirements and limiting the total grid span to 14 nm to facilitate photonic integration and simplified processing, both leading to a high yield. The LAN WDM grid also results in the lowest interoperable link budget because it is placed in the region of minimum fiber loss (for the 1310 nm window) and dispersion.

Lane	Center wavelengths	Wavelength ranges
L0	1271 nm	1264.5–1277.5 nm
L1	1291 nm	1284.5–1297.5 nm
L2	1311 nm	1304.5–1317.5 nm
L3	1331 nm	1324.5–1337.5 nm

Table 1. *CWDM optical wavelength assignments.*

Lane	Center frequencies	Center wavelengths	Wavelength ranges
L0	231.4 THz	1295.56 nm	1294.53–1296.59 nm
L1	230.6 THz	1300.05 nm	1299.02–1301.09 nm
L2	229.8 THz	1304.58 nm	1303.54–1305.63 nm
L3	229.0 THz	1309.14 nm	1308.09–1310.19 nm

Table 2. *LAN WDM optical wavelength assignments.*

Hybrid PLC DML Photonic Integrated Circuits

DML/DML Arrays

DMLs are the optical source of choice for SMF applications up to a 10 km reach and for data rates up to 10 Gb/s. These devices are available from multiple suppliers and have mature performance and reliability. For 40GE PLC integration, four single 10 Gb/s DFB lasers can be used, similar to the single 10 Gb/s DFB laser used for 10GE. It is possible to use a quad 10 Gb/s laser array for 40GE PLC integration; however, the 60 nm 40GE CWDM grid span presents manufacturing challenges. A CWDM quad laser array requires several separate growth steps, resulting in lower yield than that of four single lasers. So, although monolithic CWDM 10 Gb/s DFB laser arrays are feasible, for example, as shown in Fig. 6, at present the use of single 10 Gb/s lasers leads to lower cost PLCs.

For 100GBASE-LR4, 25 Gb/s DMLs are preferred over EMLs because of the modest dispersion requirements of the 10 km reach and the reduced chip complexity, size, and cost. Because no commercial devices are available today, device optimization and demonstration of reliable long-term operation is required. The 25 Gb/s DMLs also require the use of a thermoelectric cooler (TEC) to avoid a drop-off in efficiency and bandwidth at higher temperatures. PLC integration offers the benefit of lower power consumption through reduction of the overall passive heat load due to the smaller surface area of the integrated assembly compared to total surface area of four discrete assemblies.

The 14 nm LAN WDM grid span enables quad 25 Gb/s DFB arrays to be manufactured with a single growth step using selective area growth (SAG) techniques. Challenges in the manufacture of such DFB arrays arise from the requirement to emit different wavelengths while achieving uniformity of array performance characteristics: single-mode yield, output power, and burn in yield. This uniformity can be achieved by using quarter-wave shifted DFBs manufactured using direct e-beam grating-writing or phase-mask printing [7].

PLC WDM Multiplexer Technology

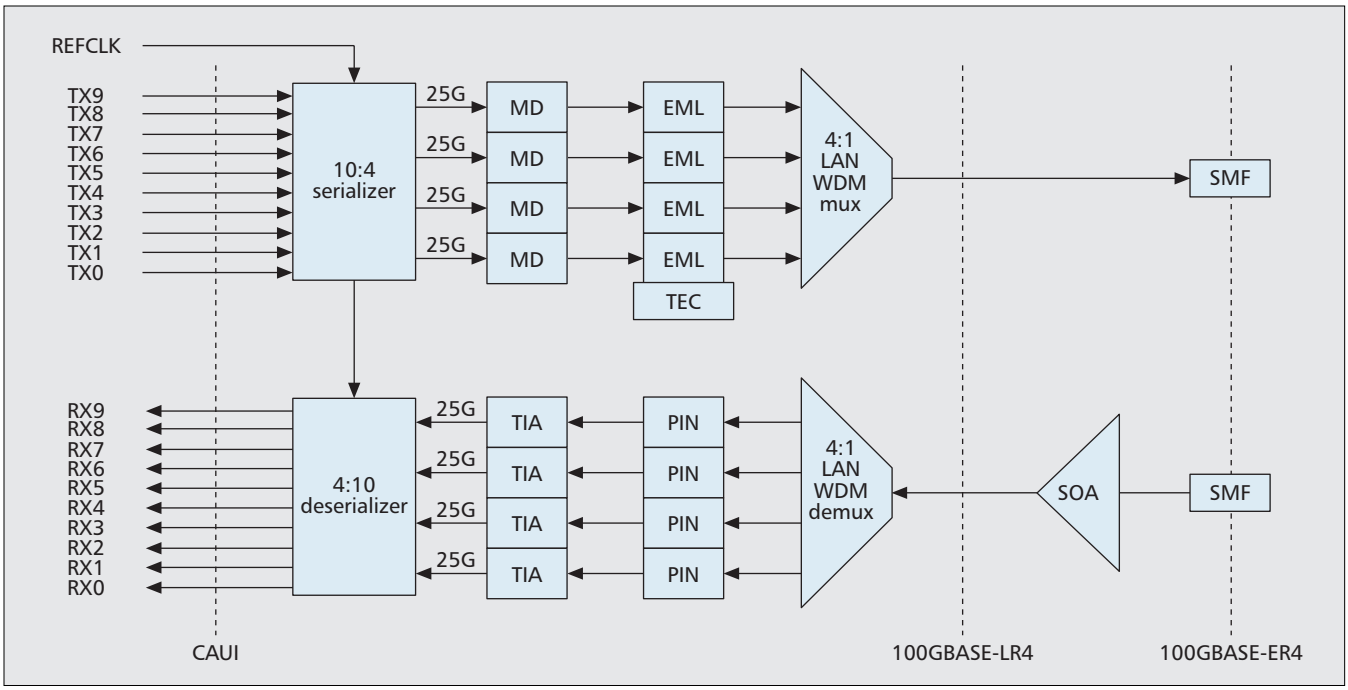
The optical power budgets of 40GE and 100GE are difficult to meet using a simple power combining for the multiplexer because of the inherent insertion loss of 6 dB for a four-channel device in addition to the laser-PLC coupling loss. Lower loss wavelength-dependent multiplexer must be used. Unlike in a power combiner, this requires the alignment of the multiplexer pass-bands to the laser wavelengths so the laser array and multiplexer must be manufactured with tight relative tolerances or must support tuning of their wavelengths relative to each other. Temperature tuning of either the laser or the multiplexer can be used to achieve this. The most common dispersive elements used for implementing PLC multiplexers are the AWG and planar Echelle grating [8]. The multiplexer performance is determined by polarization dependence, insertion loss, achievable pass-band width, and channel-to-channel isolation.

Coupling DFB Lasers to PLC

The basic challenge of PLC hybrid integration is achieving low-loss coupling between the laser and the PLC waveguide. To achieve low-loss coupling without lenses, the optical modes of the laser and PLC waveguides must be closely matched in size. For low-loss coupling with relaxed alignment tolerances, the modes should both be as large as practical, although if taken too far, angular alignment tolerances become the limiting factor.

Laser waveguides inherently have a small optical mode size in order to have a large overlap with the optical gain of the active region. A typical laser mode size is in the range of 1 to 2 μm. Optical fiber and glass-on-silicon PLCs have much larger mode sizes, in the 5 to 10 μm range, due to the smaller available refractive index step in glass. Without the use of coupling optics, coupling losses between the laser and a glass PLC waveguide can be up to 10 dB, even when perfect mechanical alignment is assumed. The mode size of silicon-on-insulator (SOI) PLC waveguides is closer to that of lasers, 3 to 5 μm, but the small alignment tolerance makes it difficult to use low-cost passive alignment of the laser.

To overcome the challenge of matching the laser-waveguide spot size to the PLC spot size, various options exist for adding waveguide structures on either the laser or the PLC side to better match the two mode field sizes. Most commonly used are waveguide taper structures that widen the laser spot size or reduce the PLC waveguide spot size [8]. Both can achieve better minimum coupling loss at the expense of more stringent mechanical alignment. In the case of the laser side taper, lateral mechanical alignment is relaxed, whereas angular alignment becomes more stringent. In the case of PLC side taper, angular alignment is more forgiving whereas lat-



■ **Figure 2.** *100GBASE-LR4 and 100GBASE-ER4 transceiver architecture. ER4 optical interface requires SOA; LR4 does not. LR4 can also use four cooled DMLs (not shown) in place of the four cooled EMLs (shown).*

eral alignment is more critical. In both cases, placement accuracies on a sub-micron scale must be achieved during laser chip attachment.

The most commonly used attachment process is the flip-chip alignment of the laser to the PLC platform [9]. Another fairly common method is the butt coupling of a laser to the PLC facet. A combination of both flip-chip coupling for the laser diodes and butt coupling to the PLC facet is reported in [10]. Lateral alignment in this case is performed by actively monitoring the coupled power and fixing the two pieces in place when maximum power is achieved. An inherent drawback of this method, if used for direct laser attachment without the flip-chip step reported in [10], is that the vertical direction is usually the most stringent with respect to alignment tolerances. Tolerances much less than 1 micron are required. A process to routinely guarantee this accuracy at the end of the attachment process is difficult to achieve.

In the case of flip-chip coupling, the laser is soldered with the active side down on the PLC to bring the two waveguides in close proximity to each other. This must be done with very high accuracy both in lateral and angular positioning. As compared to butt coupling on the PLC facet, flip-chip coupling has the benefit of relatively easy control of the relative waveguide position in the vertical dimension, based on epitaxial growth of the laser layers and only shallow etching of the PLC mounting structures. Figure 3 shows a laser flip-chipped onto a PLC with the alignment axis identified.

With respect to lateral alignment, current attachment/placement technology can achieve the required accuracy with acceptable yields for single-laser attachment by pattern recognition and passive visual alignment. This means that the laser is aligned to the PLC by matching features precisely manufactured on both chips without a requirement for active alignment between the two waveguides. For comparison, active alignment (maximizing the fiber-coupled power while the laser is switched on) is the method of choice for most optical single-channel SMF discrete transmitter assemblies.

Apart from alignment based on mechanical features (alignment marks on both the laser and the PLC), methods also are reported that use purely passive alignment where these features act as stops for vertical and lateral movement. This requires a custom design of the topography on both components and therefore limits potential sourcing of laser and PLC. Another method in the purely passive area is alignment by the solder bumps and the forces exerted through the reflow and surface tension of the solder itself. This is a very elegant method, but requires very tight process control of the soldering process and the mechanical stops to provide accurate alignment after reflow.

Independent of which technology is used, if more than one laser must be attached to a given PLC, the probability of one connection not meeting the required coupling efficiency reduces the overall yield of the product. Depending on the quality of the single attachment process, it can be beneficial to attach an array of lasers instead of single chips, reducing the number of overall attachment processes and therefore, the probability of a failed attachment due to too much insertion loss.

The challenges of the array attachment are the larger size of the array and the requirement to have multiple pads on the laser array soldered at the same time with good consistency. The handling of long laser bars is challenging because the semiconductor materials can break easily, and the bars cannot be touched in the area of

the laser facets. A long bar also must be supported evenly during soldering, or it might bend and lose vertical alignment to the PLC laser waveguide. On the other hand, some of the challenges are offset by the easier detection of the rotation angle of the bar in the visual alignment system, and therefore, much better angular alignment accuracy can be achieved than for single laser chips.

Hybrid PLC Example

The benefits and drawbacks of the various approaches lead to different PLC types for 40GE and 100GE. For 40GE PLC, the high yield of single lasers and lower yield of CWDM laser arrays, leads to the use of single DFBs as shown in Fig. 4. Because it is much easier to build laser arrays on the 100GE LAN WDM grid, the 100GE PLC uses quad DFB arrays in place of the four single DFBs shown in Fig. 4.

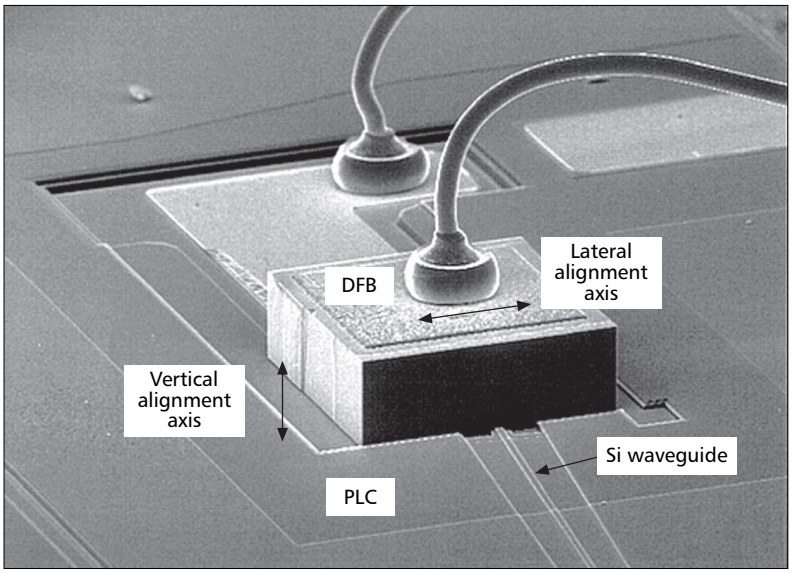


Figure 3. *Laser diode flip chipped onto a PLC, showing alignment axis.*

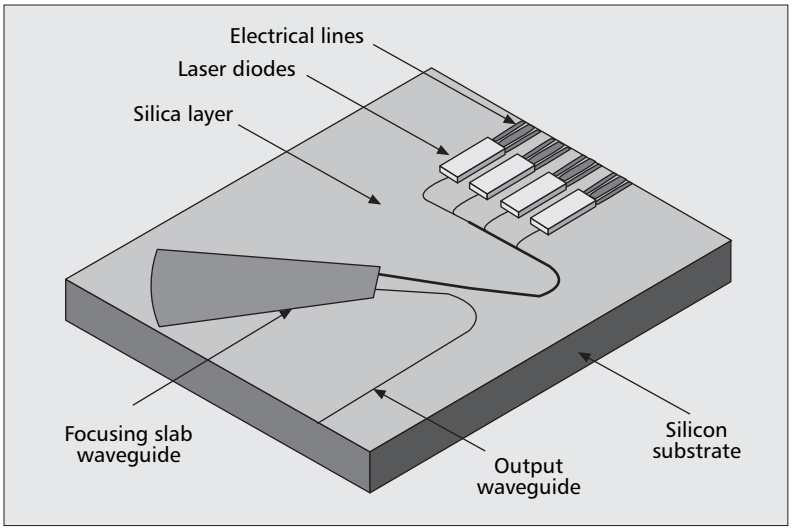


Figure 4. *PLC with four discrete DFBs (shown) for 40 Gb/s 10 km 40GBASE-LR4 applications. Quad monolithic DFB array (not shown) replaces the four discrete DFBs for 100 Gb/s 10 km 100GBASE-LR4 applications.*

Monolithic InP EML Photonic Integrated Circuits

EML Technology

Unlike the DML solution, the 25 Gb/s data rate does not require additional development because 40 Gb/s EMLs already are commercially available. As in the case of the DML array, the 100GE LAN WDM grid is wide enough to enable high DFB laser array wavelength yield, yet narrow enough to allow four EMLs to be integrated on a single monolithic InP chip within the multiple-quantum well (MQW), band-gap shift that is realizable using SAG. The SAG technique is used today in many commercial EMLs; therefore, no additional processing steps are required to produce an array of EMLs. EA modulators are simple and robust and typically have high yield. The additional modulator processing and chip area increases the requirements on the DFB laser yield in order for the PIC to be cost effective.

Multiplexer Technology

InP must be used for the quad 25 Gb/s EMLs array, but the choice of InP for the optical multiplexer function is not as obvious. Although the cost of InP is higher than that of silicon, the high index step makes it possible to design very compact AWGs. The high-index step also increases the AWG insertion loss relative to glass or silicon, but this is offset for the most part by the absence of the 3-dB or more coupling loss typical for hybrid integration. Thus, the total multiplexer losses of the PLC and PIC approaches are comparable. In addition, monolithic InP AWGs offer an important benefit in that they tune with temperature at the same rate as a DFB laser; therefore, no change in alignment between multiplexer pass-bands and laser wavelengths over temperature occur, as is the case with silica AWG. Also, because the insertion loss of a 4:1 wavelength-independent multi-mode interference (MMI) combiner is only slightly larger than what can be achieved with InP AWGs (without incurring additional yield loss due to wavelength misalignment), this is another potential approach for monolithic integration with a 25 Gb/s EML array.

Manufacturing Technology

The integration technology used to fabricate a quad 25 Gb/s EML PIC must accomplish several key goals. First, active MQW epi material with band-gaps appropriate for each element of the source array must be provided. This is easily accomplished with SAG. In the SAG technique, the laser and modulator MQW regions are grown using organo-metallic vapor phase epitaxy (OMVPE) on an InP substrate, patterned with silicon dioxide (SiO_2) stripes. The oxide results in additional diffusion of group-III elements into narrow gaps between the stripes, which increases the growth rate of the InGaAsP layers, shifts the band-gap to longer wavelength, but also makes the lattice mismatch more compressive. The band-gaps of the laser MQW in an array must be spaced by the channel spacing, $(N - 1)^{*}\Delta\lambda$ total, and the modulator MQW band-gaps must

be 30 to 50 nm less than the lasers for low on-state absorption and high off-state extinction ratio. Because the total band-gap difference between the shortest wavelength modulator and the longest wavelength laser in the EML array is only 14 nm more than is used for single EMLs, this is not an issue for 100GE PICs.

Second, low-loss coupling to the passive waveguide material used for the AWG must be provided. Many different active-passive integration techniques exist, but the etch-and-re-grow or butt-joint technique results in low loss with minimum transition length. In the butt-joint growth technique, the active layer stack is grown first on a planar substrate and then protected with a SiO_2 mask where it is required in the PIC. The exposed active layers are then etched away, and the passive waveguide layer stack is grown using OMVPE. The key to successful butt-joint integration is in the optimization of the etching and OMVPE conditions in order to produce a joint with the right vertical alignment and morphology for low-loss-mode matching between the two waveguides. Figure 5 shows a scanning electron microscope (SEM) cross-section of a high quality, active-passive butt joint.

Third, tight control of the effective index of the waveguides must be provided to minimize AWG wavelength registration losses. This is accomplished by careful calibration of the composition and thickness of the waveguide layer and using dry etching techniques for the deep-ridge waveguide to control the ridge width.

Other processing steps required for PICs, such as electrical isolation, dielectric deposition, and metallization, are the same as for single EMLs. The entire PIC process uses process equipment that is commercially available and commonly found in most InP fabrication facilities.

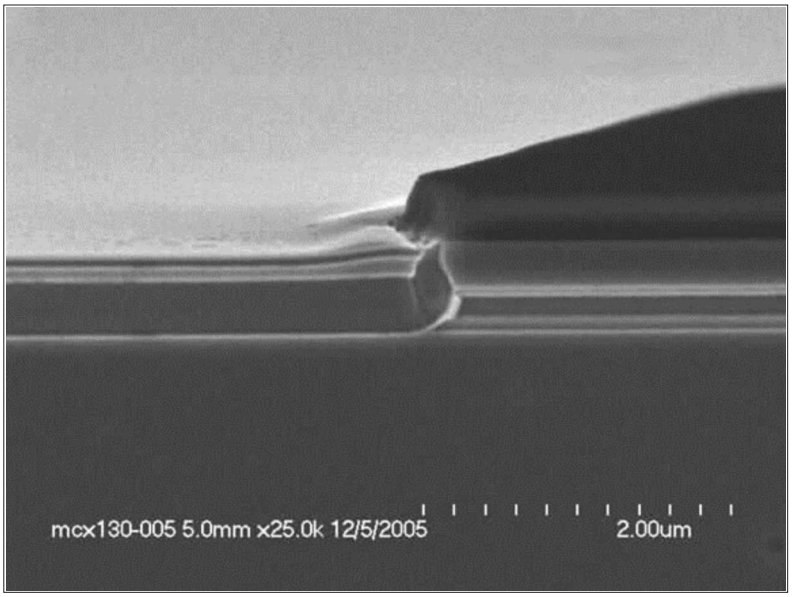


Figure 5. *Scanning electron microscope photograph of the etched and regrown butt joint between the laser MQW on the right and the passive waveguide layer on the left. The oxide mask is still in place.*

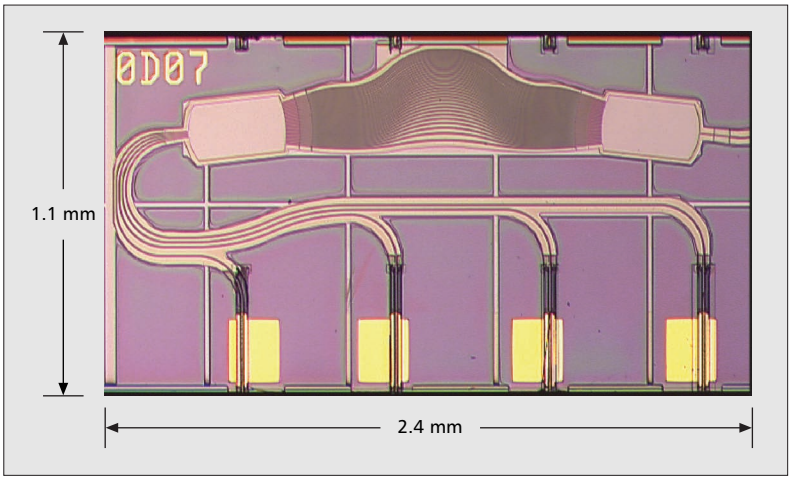


Figure 6. *Photograph of a monolithic InP PIC comprising four O-band DFB lasers and an AWG with 24.5 nm channel spacing. The chip size is 1.1 × 2.4 mm.*

Monolithic PIC Example

An example of a quad 10 Gb/s DML PIC is shown in Fig. 6. This device consists of four, directly-modulated InAlGaAs MQW DFB lasers on a 24.5 nm 10GBase-LX4 grid integrated with an InGaAsP AWG multiplexer. As discussed, new products no longer use the LX4 grid, and a 74 nm grid span presents challenges for monolithic laser array manufacturing. However, this chip was a good project for establishing and demonstrating the feasibility of the fabrication processes required for devices such as the quad 25 Gb/s EML PIC.

All of the epitaxy is performed using OMVPE. The arrays of quarter-wave shifted DFB gratings were defined using electron-beam lithography and etched into the InGaAsP grating layer using methane-hydrogen reactive ion etching (RIE). The MQW active layers for the laser array are grown with the SAG technique to shift the un-enhanced 1276 nm band-gap MQW by 24.5, 49, and 73.5 nm using successively wider pairs of SiO_2 stripes. For the quad 25 Gb/s EML PIC, SAG also is used to shift the band-gaps of the modulator MQW.

A second SiO2 mask is then used to protect the laser array while the exposed laser active layers are etched away and the bulk InGaAsP waveguide layer is re-grown in its place. After growing the p-InP cladding and p+ InGaAs cap layers, the laser ridges are fabricated using selective wet etching to produce shallow ridge waveguide lasers. Then, passive waveguides are etched through the waveguide layer using methane-hydrogen reactive ion etching (RIE) to produce a high lateral index step and smooth sidewalls. The ridges are approximately 2.2 μm wide. The waveguides are then passivated with 0.5 μm thick SiO_2, and conventional techniques are used to form the laser contacts and bonding pads. The resulting PIC is 1.1 mm wide by 2.4 μm long.

The performance of the quad 10 Gb/s DML PIC was measured at room temperature. The quarter-wave shifted DFB arrays had good yield and were within ±1.5 nm of the target grid. The AWG 1 dB down pass-band width was 10 nm and the channels were within ±5 nm of the tar-

The IEEE 802.3ba 40 Gb/s and 100 Gb/s SMF optical interface standards offer ideal applications for developing integrated optical transmitter circuits because they require a moderate number of optical components and in the future, will require low cost, small size, and reduced power consumption.

get grid. The total insertion loss of the AWG was determined to be 6.5 dB, which is comparable to the total insertion plus coupling loss of a hybrid PLC. A major contributor is the waveguide bending loss between the lasers and AWG, which was estimated to be 3 dB. This is easily addressed by the use of slightly larger bend radii, but at the expense of chip size. Typical output power coupled into single-mode fiber was –7 dBm per channel at a bias current of 50 mA.

The additional process fabrication steps required for a quad 25 Gb/s EML PIC are already standard for EMLs, such as electrical isolation between the laser and modulator, and low-k dielectrics for the modulator bonding pad. The modulators themselves are high-yield components relative to the DFB lasers, so they are not expected to cause additional yield issues. The loss budget for 100GE-LR4 requires –1 dBm average power per channel, so development to further minimize waveguide, bending, and AWG losses is important. Additional studies must be conducted to determine the lowest cost multiplexer approach: AWG or MMI.

Conclusions

Component and attachment technologies are available today to enable efficient high-yield manufacturing of hybrid and monolithic optical integrated circuits. The recently adopted IEEE 802.3ba 40 Gb/s and 100 Gb/s SMF optical interface standards offer ideal applications for development of integrated optical transmitter circuits because they require a moderate number of optical components and in the future, will require low cost, small size, and reduced power consumption. This combination of factors will lead to significant investment in commercial, photonic integration technology and infrastructure by the optics industry.

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References

[1] T. L. Koch and U. Koren, "Semiconductor Photonic Integrated Circuits," *J. Quantum Electronics*, vol. 27, no. 3, 1991, pp. 641–53.

[2] L. A. Coldren, "InP-Based Photonic Integrated Circuits," *Conf. Lasers Electro-Optics*, paper CTuBB1, 2008.

[3] IEEE 802.3ba 40 Gb/s and 100 Gb/s Ethernet Task Force Public Area; http://www.ieee802.org/3/ba/index.html

[4] M. Aoki *et al.*, "InGaAs/InGaAsP MQW Electro-Absorption Modulator Integrated with a DFB Laser Fabricated by Band-Gap Energy Control Selective Area MOCVD," *J. Quantum Electronics*, vol. 29, no. 6, 1993, pp. 2088–96.

[5] D. F. Welch *et al.*, "Large-Scale InP Photonic Integrated Circuits: Enabling Efficient Scaling of Optical Transport Networks," *IEEE J. Selected Topics Quantum Electronics*, Jan.–Feb. 2007, pp. 22–31.

[6] J.-O. Wesstrom *et al.*, "State-of-the-Art Performance of Widely Tunable Modulated Grating Y-Branch Lasers," *Optical Fiber Commun. Conf.*, paper TuE2, 2004.

[7] L. J. P. Ketelsen *et al.*, "Multiwavelength DFB Laser Array with Integrated Spot Size Converters," *J. Quantum Electronics*, vol. 36, no. 6, 2000, pp. 641–48.

[8] A. Himeno *et al.*, "Silica-Based Planar Lightwave Circuits," *IEEE J. Selected Topics Quantum Electronics*, Nov.–Dec. 1998, pp. 913–24.

[9] K. Kato and Y. Tohmori, "PLC Hybrid Integration Technology and Its Application to Photonic Components," *IEEE J. Selected Topics Quantum Electronics*, Jan.–Feb. 2000, pp. 4–13.

[10] Y.-T. Han *et al.*, "Fabrication of a TFF-Attached WDM-Type Triplex Transceiver Module Using Silica PLC Hybrid Integration Technology," *J. Lightwave Tech.*, vol. 24, no. 14, Dec. 2006, pp. 5031–38.

Biographies

Chris Cole [SM] (chris.cole@finisar.com) received a B.S. in aeronautics and astronautics and B.S. and M.S. degrees in electrical engineering from the Massachusetts Institute of Technology. He is a director at Finisar Corp., Sunnyvale, California. He now manages the development of 40 Gb/s and 100 Gb/s LAN and WAN optical transceivers at Finisar (which acquired his previous company, Big Bear Networks). At Hughes Aircraft Co. (now Boeing SDC) and then M.I.T. Lincoln Laboratory, he contributed to multiple imaging and communication satellite programs. Later, he consulted on telecom ICs for the Texas Instruments DSP Group and Silicon Systems Inc. (now Teridian). At Acuson Corp. (now Siemens Ultrasound), he was one of the architects of the Sequoia coherent imaging ultrasound platform, where he was also director of hardware and software development groups. As a principal consultant with the Parallax Group, he carried out signal processing analysis and product definition for several imaging and communication systems. He now manages the development of 40 Gb/s and 100 Gb/s LAN and WAN optical transceivers at Finisar (which acquired his previous company, Big Bear Networks).

Bernd Huebner (bernd.huebner@finisar.com) holds an M.S. in physics from Technische Universität, Darmstadt, Germany and a Ph.D. in physics from Julius Maximilians Universität, Würzburg, Germany. He is a manager of OSA engineering at Finisar. At Deutsche Telekom, he researched fabrication and characterization of low-dimensional compound semiconductor structures and DFB lasers with spot size conversion. Then at Aifotec AG, he was responsible for the development of an FGL module based on a hybrid photonic platform, which included designing lasers and manufacturing processes. He now manages the development of OSA technologies for FTTH, 10 Gb/s, 40 Gb/s, and 100 Gb/s transceivers at Finisar.

John E. Johnson [SM] (jjohnson@cyoptics.com) received a B.S.and Ph.D. in electrical engineering from Cornell University. He is a manager of photonics design at CyOptics, Inc. He worked for three years at National Semiconductor in analog IC manufacturing. He then joined AT&T Bell Laboratories (later Lucent Technologies Bell Laboratories), then Agere Systems Research, and then TriQuint Semiconductor, where he led research into a broad range of InP photonic integrated circuits, including EMLs, EA-modulated and CW high-power tunable DBR lasers, spot-size converted lasers, and SOAs operating at bit rates up to 160 Gb/s. This included bringing to market award-winning EML and tunable transmitter products. Then, at T-Networks (later Apogee Photonics, now part of CyOptics after an acquisition), he became the manager of photonics development, responsible for the design and manufacturing ramp-up of several 10 Gb/s and 40 Gb/s EA-modulated devices. He now leads InP chip design and product development. He is the author or co-author of more than 50 peer-reviewed papers and 13 patents (issued and pending).