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INNOVATORS IN INTEGRATION

SSI K224 Single Chip V.22 bis Modem

(Availability: Fall 1986)

Preliminary Data Sheet

INTRODUCTION

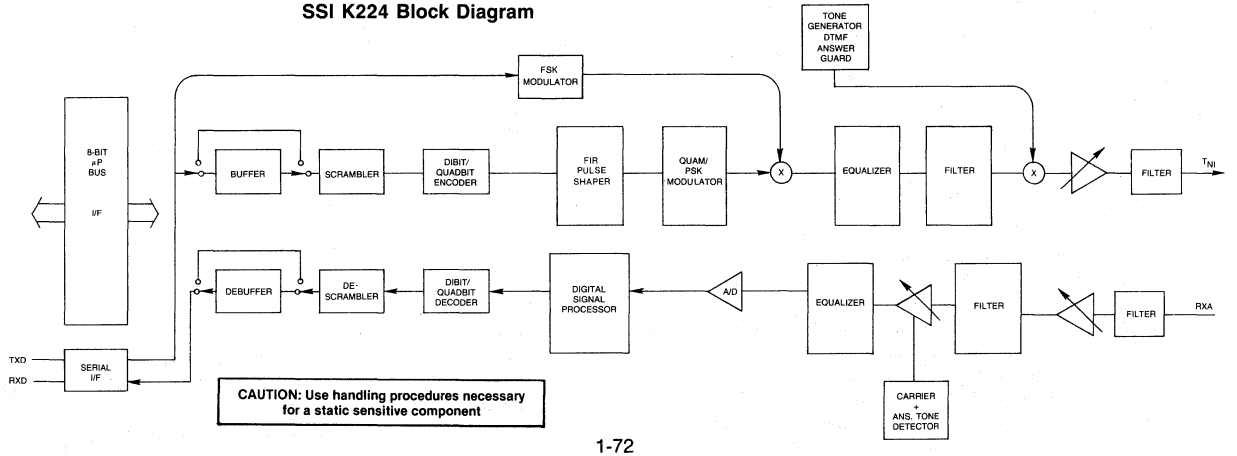
The SSI K224 is a highly integrated single-chip modem I.C. which provides the functions needed to construct a V.22 bis compatible modem, capable of 2400 BPS full-duplex operation over dial-up lines. Using an advanced CMOS process that integrates analog, digital signal processing, and switched-capacitor array functions on a single substrate, the SSI K224 offers excellent performance and a high level of functional integration in a single 28 pin DIP configuration. The K224 provides the QAM, PSK and FSK modulator/demodulator functions, call progress and handshake tone monitors, test modes, and a tone generator capable of producing DTMF, answer, and simultaneous 550 and 1800 Hz guard tones required for European applications. This device supports all V.22 bis, V.22, V.21, Bell 212A, and Bell 103 modes of operation, allowing both synchronous and asynchronous communication. The K224 is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial command bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only. The K224 is pin and software compatible with the SSI K212 and K222 one-chip modem I.C.'s, allowing system upgrades with a single component change.

The K224 is ideal for use in either free standing or integral system modem products where full-duplex 2400 BPS data communications over the 2-wire switched telephone network is desired. It's high functionality, low power consumption, and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level convertors for a typical system. Adaptive equalization assures the user of optimum performance over all line conditions when operating in the QAM and PSK modes.

FEATURES

- **One-chip multi-mode V.22 bis/Bell 212A compatible modem**
- **Full duplex operation at 0-300, 1200, and 2400 BPS**
- **FSK (300 BPS), PSK (1200 BPS), or QAM (2400 BPS) encoding**
- **Pin and software compatible with SSI K212 and K222 1-chip modems**
- **Interfaces directly with standard microprocessors (8048), 80C51 typical)**
- **Serial (22 Pin DIP) or parallel microprocessor bus (28 pin DIP) for control**
- **Serial port for data transfer**
- **Maskable interrupts**
- **Selectable asynch/synch and scrambler/descrambler functions**
- **All synchronous and asynchronous operating modes**
- **Adaptive equalization for optimum performance over all lines**
- **Programmable transmit gain (15dB, 1dB steps), selectable receive boost (+12dB)**
- **Call progress, carrier, answer tone, and signal quality monitors**
- **DTMF and guard tone generators**
- **Test modes available — ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **Space efficient 22 and 28 pin DIP packages**
- **CMOS technology for low power consumption (120 MW) with power down mode (30 mW)**
- **Single +12 volt supply**
- **TTL and CMOS compatible inputs and outputs**

SSI K224 Block Diagram



OPERATION

General

The SSI K224 was designed to be a complete V.22 bis compatible modem on a chip. It requires only the addition of a control microprocessor, RS-232, and a phone line interface to design a complete modem. As many functions as possible were included in order to simplify implementation into typical modem designs. In addition to the basic 2400 BPS QAM, 1200 BPS PSK and 300 BPS FSK modulator/demodulator sections, the device also includes synch/asynch converters, scramber/descrambler, call progress tone detect, and DTMF tone generator capabilities. All V.22 bis and Bell 212A modes are supported (synchronous and asynchronous) and test modes are provided for diagnostics. Most functions are selectable as options and logical defaults are provided when override modes are chosen. The device can be directly interfaced to a microprocessor via its 8-bit multiplexed address/data bus for control and status monitoring. Datacommunication takes place through a separate serial port.

QAM Modulator/Demodulator

The SSI K224 encodes incoming data into quadbits represented by 16 possible signal points with specific phase and amplitude levels. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited telephone network. The modulator transmits this encoded data using either a 1200 Hz (originate mode) or 2400 Hz (answer mode) carrier. The demodulator reverses this procedure but also recovers a data clock from the incoming signal. Adaptive equalization corrects for varying line conditions by automatically changing filter parameters to compensate for those line characteristics.

PSK Modulator/Demodulator

The K224 modulates a serial bit stream into dibit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A/V.22 standard. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire PSTN line. Transmission occurs on either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into dibits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The K224 uses a phase locked loop coherent demodulation technique that offers inherently better performance than typical DPSK demodulators used by other manufacturers. Adaptive equalization is also used in PSK modes for optimum operation with slowly varying line conditions.

FSK Modulator/Demodulator

The FSK modulator frequency modulates the analog output signal using two discrete frequencies to represent the binary data. The Bell 103 standard frequencies of 1270 Hz and 1070 Hz (originate mark and space) and 2225 Hz and 2025 Hz (answer mark and space) are used when this mode is selected. V.21 frequencies are used when this mode is selected. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are bypassed in the FSK modes.

Passband Filters and Equalizers

A high and low band filter is included to shape the amplitude and phase response of the transmit signal and provide compromise delay equalization and rejection of out of band signals in the receive channel. Amplitude and phase equalization is necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering corresponds to a 75% square root of raised Cosine frequency response characteristic.

Asynchronous Mode

The asynchronous mode is used for communication with asychronous terminals which may communicate at 1200 BPS +1%, −2.5% even though the modem's output is limited to 1200 BPS ±.01%. When transmitting in this mode the serial data on the TxD input is passed through a rate convertor which inserts or deletes stop bits in the serial bit stream in order to output a signal that is exactly 1200 BPS ±.01%. This signal is then routed to a data scrambler (following the CCITT V.22 algorithm) and into the analog PSK modulator where dibit encoding results in a V.22 bis or Bell 212A standard output signal. Both the rate convertor and scrambler can be bypassed for handshaking, FSK, and synchronous operation. The device recognizes a break signal and handles it in accordance with Bell 212A specifications. Received data is processed in a similar fashion except that the rate convertor now acts to reinsert any deleted stop bits and output data to the terminal at no greater than 1219 BPS. An incoming break signal will be passed through without incorrectly inserting a stop bit.

Synchronous Mode

Synchronous operation is possible only with the QAM or PSK modes. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TxD must be valid on the falling edge ot TxCLK. Receive data at the RxD pin is clocked out on the rising edge of RxCLK. The asynch/synch convertor is bypassed when synchronous mode is selected and data is transmitted out at essentially the same rate as it is input.

Parallel Bus Interface

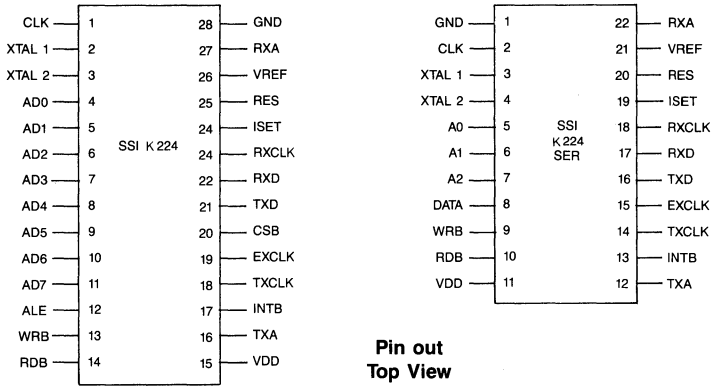
Six 8-bit registers are provided for control, option select, and status monitoring. These registers are addressed with the A0, A1, and A2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as six consecutive memory locations. Five control registers are read or write memory. The status detect register is read only and cannot be modified except by modem response to monitored parameters.

Serial Command Interface

The serial command mode allows access to the K224 control and status registers via a serial command port (22 pin version only). In this mode the A0 and A1 lines provide register addresses for data passed through the data pin under control of the RD and WR lines. A read

operation is initiated when the RD line is taken low. The next eight cycles of ExCLK will then transfer out eight bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of ExCLK. WR is then pulsed low and data transfer into the selected register occurs on the rising edge of WR.

Preliminary Pin Configuration



Pin out
Top View