Kodiak OC-768 / STM-256 Short Reach 40Gb/s Electro-Optical Transponder (BBTR4005)

(with integrated Clock & Data Recovery, Clock Synthesis and Multiplexer / Demultiplexer)

Preliminary Specifications (updated 7/9/2003) Rev 0.99e
Contact support@bigbearnetworks.com for support

Features

- Electro-optical transponder operating at 40 Gb/s
- Supports OC-768 SONET and STM-256 SDH
- 16-channel 2.488 Gb/s mux /demux
- Integrated Clock Multiplication Unit
- High-performance 40Gb/s Clock & Data Recovery
- High-performance photo-receiver
- 1.5um CW Laser Source (C-band compatible)
- Optimized Modulator & Driver
- Common form factor for short reach, intermediate reach and long reach applications
- Internal protection permits any power-up sequence
- Extensive Control and Monitoring Capabilities
  - Transmit & Receive Monitors
  - Transmitter Laser Disable Input
- Operates with Standard Supply Voltages
- Compatible with Applicable Industry Standards
  - OIF-SFI5-01.0 / OIF-SXI5-01.0
  - ITU G.693, 2km links (VSR2000-3R2, 3R3 & 3R5)
  - ITU G.8251

Applications

- Cross-office Telecommunication & High-speed Data Communication Applications
- Metropolitan & Regional Area Networks, Inter- / Intra-office SONET/SDH Systems

General Description

The Kodiak transponder performs the complete parallel electrical to serial optical conversion along with the required high-speed clock generation, clock and data recovery and associated 'care and feeding' of the electro-optical components. System designers are freed from the ultra-high speed design challenges of the 40Gb/s interface. The transponder offers the highest level of integration with the industry's smallest form factor package for a complete 40Gb/s interface, making it an ideal solution for time-to-market design strategies for telecommunication applications. The electrical data interface consists of 16 differential lines of data at 2.488 Gb/s for both transmit and receive directions. The optical interface consists of a 39.813 Gb/s optical bit-stream that can transport through lengths up to 2 km of single-mode fiber.

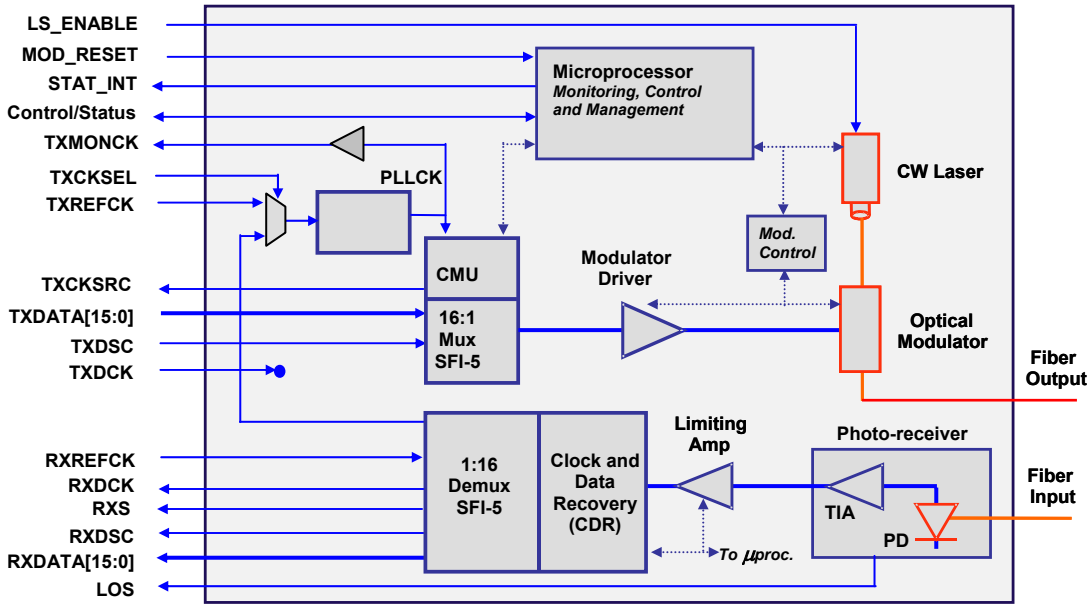


Figure 1 Transponder Block Diagram

Block Diagram Description

Figure 1 depicts a simplified block diagram of the Kodiak transponder. This bi-directional device provides a SONET/SDH compliant electro-optical interface between an OC-768/STM-256 optical signal and the electrical physical layer. The transponder operates at the standard SONET/SDH rate of 39.81Gb/s. The transponder contains a 40Gb/s optical transmitter and a 40Gb/s optical receiver, as well as the electronics required to multiplex and de-multiplex sixteen 2.488Gb/s electrical channels. Clock multiplication, clock and data recovery, and channel de-skew / alignment circuitry are embedded within the transponder.

In the transmit direction, sixteen electrical CML data channels at 2.488Gb/s are multiplexed into an optical signal at 39.813Gb/s, then launched onto an attached optical fiber pigtail. An internal reference signal at the operating rate (39.813GHz) is phase-locked to an external data timing reference clock, operating at either 1/64 or 1/16 of the operating rate, i.e. 622 MHz, or 2.488 GHz. The optical transmitter is provided by a 1.5um cooled DFB laser. The optical output signal is SONET and ITU compliant for OC-768/STM-256 applications to the extent that the respective industry specifications have been completed.

In the receive direction, the transponder receives a 39.813Gb/s optical signal, converts it to an electrical signal, extracts a clock then de-multiplexes the data into sixteen differential CML data channels at 2.488Gb/s. The optical receiver utilizes an InGaAs/InP PIN photo-detector and high performance trans-impedance amplifier.

Kodiak Transponder Product Line

The optical transmitter parameters of the Kodiak transponder are optimized for the particular SDH/SONET link characteristics in which it is to operate. Three distinct span lengths can be accommodated within the Kodiak product family (nominally 2km, 40km and 80km), providing a single active device footprint for accommodating applications ranging from intra-office at 2km to regional-based interconnects at 80km. This specification covers the short reach (SR) Kodiak Transponder operating at the standard 'non-FEC' rate of 39.8131 Gb/s. Contact Big Bear Networks for a detailed set of specifications and availability information for Transponders targeted at other operating distances and rates.

Functional Description

Transmitter

The high-speed multiplexer block shown in *Figure* 1 and *Figure 2* latches the data from the sixteen 2.488 Gb/s channels, provides the channel de-skew functions, and performs the required parallel-to-serial conversion. The FIFO input latches the data from the TXDATA_P/N [15:0]. Refer below for a detailed treatment of the Transponder / SONET Framer Interface functionality. The serialized data is shifted out of the high-speed multiplexer at the transmit serial clock rate of 39.813 Gb/s to the optical modulator driver.

The ultra-high speed modulator driver provides amplification of the 39.813 Gb/s signal to the high-drive levels required by the optical modulator. The characteristics and capabilities of the driver are matched to the particular optical modulator embedded within the Kodiak Transponder to achieve optimum transmitter performance.

The integrated electro-optic modulator imposes the 40 Gb/s data signal onto CW light from a single mode semiconductor laser. The modulator is specifically designed for the 1550nm window, external amplitude modulation application of the 40G Kodiak transponder. The transmitter has a cooled DFB laser as the optical element and operates nominally in the 1530 – 1565 nm range.

Receiver

The optical receiver of the Kodiak transponder has a high-speed InGaAs/InP PIN photo-detector and a wide-band trans-impedance amplifier (TIA), which are optimized for the particular fiber link characteristics in which it was designed to operate. The receiver converts the incident optical power to a photocurrent via the high-performance PIN photo-detector. The detected serial data output of the Kodiak receiver is connected to a limiting amplifier / clock and data recovery (CDR) sub-assembly, which extracts the 39.813 GHz clock signal and recovers the data stream.

This recovered serial bit clock signal and the retimed serial data signals are presented to the 16-bit de-multiplexer, which performs the serial-to-parallel conversion and interface functionality required for the system-side device. Refer to the Transponder / SONET Framer Interface section below for specific functional characteristics of this interface block.

Transponder / SONET Framer Interface

The following functional description provides the details of the 16-bit interface from the system-side ASIC device (typically a SONET/SDH framer) to the Kodiak Transponder. The Kodiak transponder complies with the Optical Internetworking Forum (OIF) Physical & Link Layer SFI-5 and SxI-5 interface implementation specification documents.

Figure 2 below shows a logical model of the Transmit interface in the Kodiak Transponder. Data on the Transmit Data bus (TXDATA[15:0]) is conditioned by the Phase Detector Units (PDU), which tracks the center of

the “eye” for each bit. Data from each bit lane is written into an associated re-timing buffer. Data from the re-timing buffer associated with TXDATA[15] is transmitted first onto the fiber while data that is associated with TXDATA [0] is transmitted last. The re-timing buffers acts as a set of FIFOs to bridge between the Transmit interface timing domain and the optical Transmit timing domain. The re-timing buffers absorb the allowed skew between the bit lanes.

The Kodiak Transponder monitors the Transmit Deskew Channel (TXDSC) for the reference data sourced by the system-side ASIC. It adjusts the delay of each TXDATA[15:0] signal, on a unit interval by unit interval basis, such that the delay from source device to the output of the re-timing buffers at the Transponder is identical for all 16 TXDATA signals. When the skew of all 16 data channels is compensated and locked, the TX_OOA alarm is removed. The Deskew algorithm continues to operate after the TX_OOA is removed. Under normal circumstances, the interface operates continuously with skew being monitored, and the TX_OOA alarm remains off. If failure of the Deskew algorithm occurs, and any of the 16 channels fall out of lock, then the TX_OOA alarm is enabled. TX_OOA is an I^2C alarm.

The function of the Deskew Controller block is to recognize the framing bytes and header bytes in the Deskew Channel TXDSC, to identify the start of the reference data that is replicated from each of TXDATA[X]. Each of the TXDATA[X] channels is then compared with the sampled data in the Deskew Channel in turn. The Deskew Controller performs a pattern match between the replicated data in TXDSC with the original data in the corresponding TXDATA[X] signal. Where there is a match, the relative delay of TXDATA[x], in relation to TXDSC, is found. It is possible to measure how many bit periods of skew there are on each channel. This information is used to compensate for the skew by adjusting the delay elements specific to each channel.

A delay chain is associated with each interface signal that allows the Deskew Controller to use the set of 16 relative delays to compensate for the skew in the TXDATA interface and to reconstruct the original alignment of the Transmit data TXDATA[15:0].

The out-of-alignment alarm (TX_OOA) is set if a match has not been found on any of the 16 data channels. When a data match has been found on all 16 data channels, and stable skew data derived, then the Deskew algorithm is considered locked, and the TX_OOA is cleared. Skew measurements are monitored continuously, and the TX_OOA alarm remains cleared as long as consistent skew data is generated.

Figure 3 below shows a logical model of the Receive interface in the Kodiak Transponder. Data is striped across the 16 bit lanes of the Receive Data bus (RXDATA[15:0]) in a round-robin fashion. The first bit received is written into the re-timing buffer associated with RXDATA[15] and the last into that associated with RXDATA[0]. The re-timing buffers act as a set of FIFOs to bridge between the optical timing domain and the Transmit interface timing domain.

RXDSC replicates the data sent on each signal of the Receive Data bus RXDATA[15:0] cyclically. The framing pattern generator is chosen first to insert the framing pattern of two A1 (F6 Hex) and two A2 (28 Hex) bytes and 4 bytes of expansion header (EH1 to EH4 are each currently set to 1010 1010 pattern when idle; their use is for further study). Then, each RXDATA[X] signal is sampled, in turn, for 64 bit times (8 bytes). Sampling begins with RXDATA[15] and ends with RXDATA[0]. After all the data lanes have been sent, a new reference frame is initiated on RXDSC and the process continuously repeats.

Table 1 below shows a reference frame on the Receive Deskew Channel (RXDSC). The 16 sets of data sample bytes are copied from the Receive Data bus RXDATA[15:0] starting with bit 15 RXDATA[15] and ending with bit 0 RXDATA[0]. In Table 1, transmission is from left to right and top to bottom.

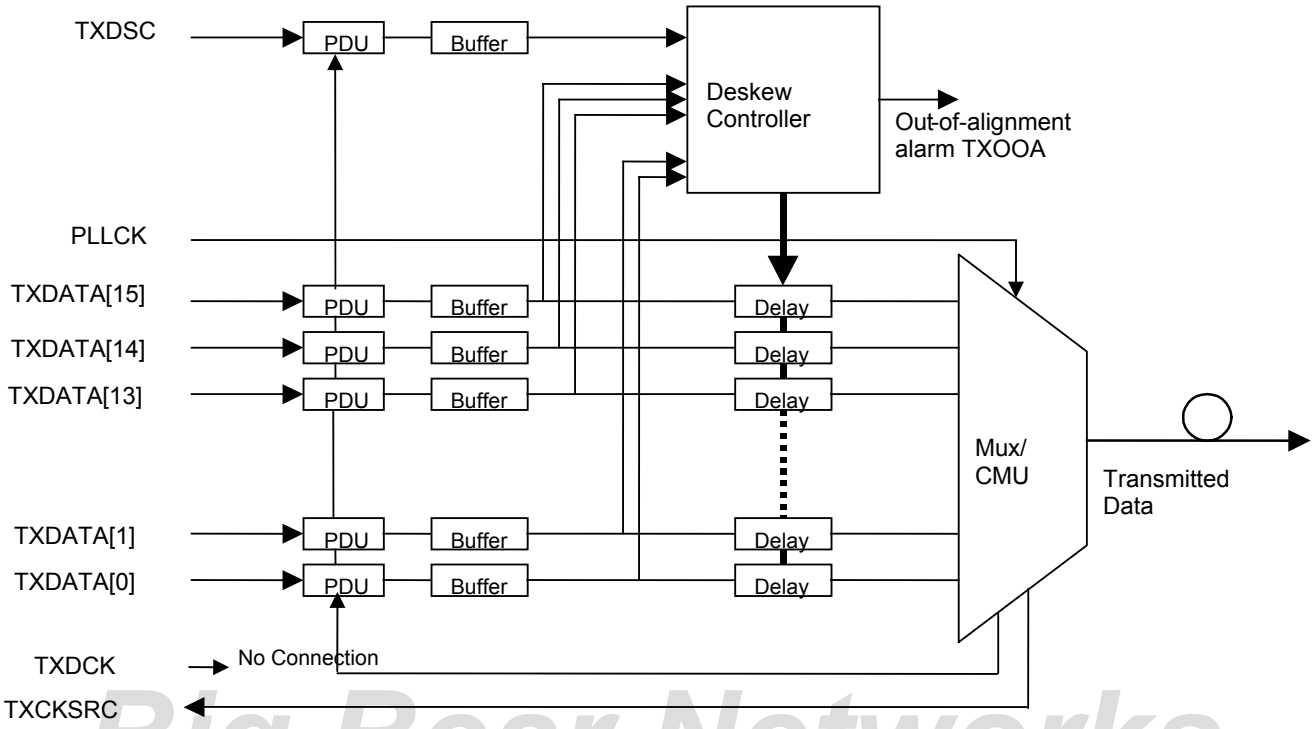


Figure 2 Transmit Multiplexer Interface

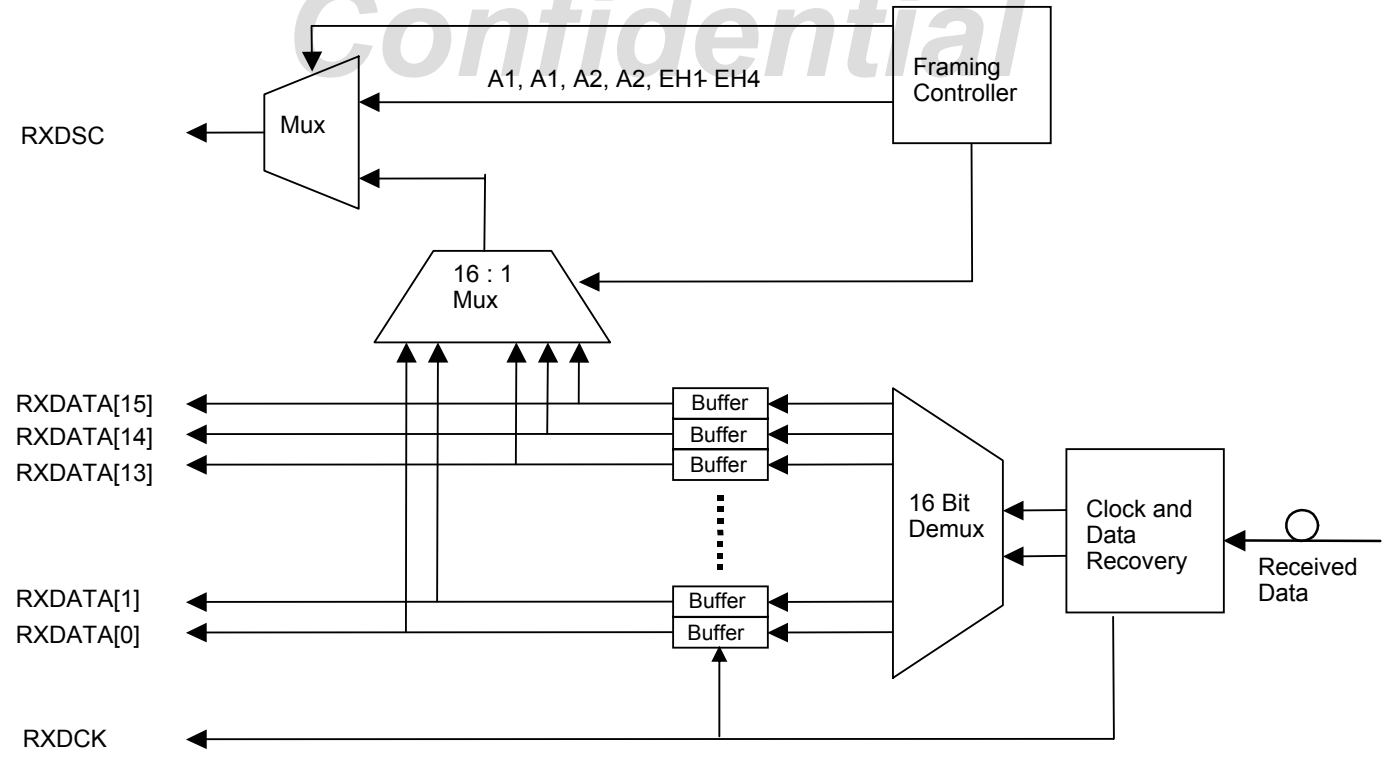


Figure 3 Receive Demultiplexer Interface

Table 1 Reference Frame on RXDSC

Bit Time	Value	Value	Value	Value	Comments
1 - 32	A1 1111 0110	A1 1111 0110	A2 0010 1000	A2 0010 1000	Framing bytes
33 - 64	EH1 1010 1010	EH2 1010 1010	EH3 1010 1010	EH4 1010 1010	Expansion Header bytes For Future Use
65 - 96	RXDATA[15] Bits 1 - 8	RXDATA[15] Bits 9 - 16	RXDATA[15] Bits 17 - 24	RXDATA[15] Bits 25 - 32	64 consecutive bits from RXDATA[15]
97 - 128	RXDATA[15] Bits 33 - 48	RXDATA[15] Bits 41 - 48	RXDATA[15] Bits 49 - 56	RXDATA[15] Bits 57 - 64	
129 - 160	RXDATA[14] Bits 1 - 8	RXDATA[14] Bits 9 - 16	RXDATA[14] Bits 17 - 24	RXDATA[14] Bits 25 - 32	64 consecutive bits from RXDATA[14]
161 - 192	RXDATA[14] Bits 33 - 48	RXDATA[14] Bits 41 - 48	RXDATA[14] Bits 49 - 56	RXDATA[14 Bits 57 - 64	
193 - 1024					64 consecutive bits from each of RXDATA[13] to RXDATA[1]
1025 - 1056	RXDATA[0] Bits 1 - 8	RXDATA[0] Bits 9 - 16	RXDATA[0] Bits 17 - 24	RXDATA[0] Bits 25 - 32	64 consecutive bits from RXDATA[0]
1057 - 1088	RXDATA[0] Bits 33 - 48	RXDATA[0] Bits 41 - 48	RXDATA[0] Bits 49 - 56	RXDATA[0 Bits 57 - 64	

Timing & Clocking

Clock timing from the system side to the transponder is provided via TXREFCK and RXREFCK. The TXREFCK and RXREFCK inputs must be generated from a source that has a frequency accuracy of equal or better than the value stated in Table 12. In order for the internally generated Transmit clock frequency to have the required accuracy for operation in a SONET/SDH system, TXREFCK must strictly meet these specifications. A lower accuracy clock source may be used in applications less demanding than SONET/SDH. Additionally, in order to meet the SONET/SDH jitter specifications, the maximum Transmit reference clock jitter must be guaranteed over the 20 kHz to 320 MHz bandwidth, so that the PLL clean-up circuitry can operate properly. For details of the reference clock jitter requirements, see Table 12.

In addition to the use of TXREFCK as the clock source the transponder can also be operated using the recovered clock from the receive chain to provide the transmit clock. This configuration would be used when operating in a loop-through mode. The choice of clock source is controlled in two ways: by the hard wired pin TXCKSEL and by the I^2C command register TxLINETIMESEL. For futher detail see the I^2C command list in section *A.3.1.1.1 Set TX Command Register* of Appendix A. Nominally TXREFCK can be either at the data rate or at one quarter of the data rate of the SFI-5 TXDATA. The TXREFCK data rate is selected using the I^2C command TxREFSEL. [Note: the rate select feature may not be available in all Transponders]. TXCKSRC is a Transponder derived source clock that is provided for use by the system side ASICs. The framer/FEC interfacing to the module must use TXCKSRC provided by the module in order to meet the jitter and wander specifications specified in the SxI-5 implementation agreement.

Monitoring and Control Functions

The Kodiak Transponder contains an on-board micro-controller, which provides a module management interface as well as performing additional housekeeping functions for the Transponder. The management interface is accessed via an I^2C bus, which is made available via two pins on the Transponder connector. Refer to *Table 14 I2C Electrical Characteristics (DC)* and *Table 15 I2C Electrical Characteristics (AC)* for the detailed electrical specifications for the I^2C interface. A three bit address I2CADDR[2:0] selects the transponder. The Kodiak Transponder operates as an I^2C bus slave. In the event of an alarm condition the transponder notifies the system that an alarm has occurred via the pin ALM_INT. The system can then determine the exact nature of the alarm by a request through the I^2C bus. A configurable hard-wire alarm is also available through pin CFG_ALM.

The transponder occupies one fixed address in the I^2C space. The specific command protocol for the I^2C interface is provided in Appendix A.

Pin Descriptions

Table 2 SerDes / Framer Interface – 16 x 2.488Gb/s Interface

Name	I/O	Type	Description
RXDATA[15:0]_P/N	O	DCML	**Receive Data**. The Received Data signals (RXDATA) carry data from the transponder deserializer to the system ASIC. Serial optical data is striped onto RXDATA[15:0] in a round-robin fashion. RXDATA[15] contains the first bit received while RXDATA[0] the last bit received. RXDATA[15] contains the first bit of the first byte received while RXDATA[0] contains the last bit of the second byte received. RXDATA is frequency locked to RXDCK with unspecified static phase offset.
RXDSC_P/N	O	DCML	**Receive Deskew Channel.** The Receive Deskew Channel (RXDSC) signal provides reference data to enable skew measurements of the Receive data bus (RXDATA[15:0]). RXDSC is a 2.488 Gb/s stream. RXDSC contains reference frames consisting of 4 framing bytes, 4 bytes of expansion header, and 16 sets of 8-byte samples of each signal on the Receive data bus (RXDATA[15:0]). Samples are taken from the Receive data bus in a round-robin fashion, starting with RXDATA[15] and ending with RXDATA[0]. RXDSC is frequency locked to RXDCK with unspecified static phase offset.
RXS	O	LVTTL	**Receive Status.** The Receive Status (RXS) signal carries status from the Transponder to the system ASIC. An RXS alarm indicates that RXDCK and RXDATA are not derived from the optical receive signal. RXS is an asynchronous signal which is 'active high': "0"=Normal Op., "1"=Alarm RXS is detected in hardware and is asynchronous with respect to the micro-controller. Two conditions will cause the RXS alarm to trigger: 1) When the CDR VCO frequency is greater than 1000ppm from the input reference clock RXREFCK. Under this condition the VCO will perform a relock search by sweeping frequency. This search may result in the RXS alarm toggling on and off until a valid lock is obtained (at which point the alarm will be off). 2) RXS will also trigger if the input optical power is below -10.5dBm (with 1dB hysteresis). Under this condition the CDR VCO will lock to RXREFCK. The response time of RXS is given below in Table 4.
RXDCK_P/N	O	DCML	**Receive Data Clock**. The Receive Data Clock (RXDCK) signal provides timing reference for the Receive data path signals (RXDATA, RXDSC). RXDCK is nominally a 50% duty cycle clock with a frequency that is one-quarter of the data bit rate of RXDATA and RXDSC. RXDCK is frequency locked to these signals. Static phase offset between RXDCK and RXDATA, RXDSC is unspecified. RXDCK tracks the frequency of the CDR VCO. Therefore if RXS triggers while the input power is below -10.5 dBm then RXDCK will lock to RXREFCK. If RXS triggers with input power above -10.5 dBm then RXDCK will sweep in frequency around RXREFCK.
RXREFCK_P/N	I	Diff LVPECL	**Receive Reference clock.** (RXREFCK) signal is a low jitter input reference that provides timing for the Clock and Data Recovery (CDR) loop. Same frequency as TXREFCK.
TXDATA[15:0]_P/N	I	DCML	**Transmit Data.** The Transmit Data (TXDATA[15:0]) signals carry data from the system-side ASIC (e.g. SONET Framer) to the transponder serializer. Data on TXDATA[15:0] are placed on the transmit optical stream in a round-robin fashion. TXDATA[15] contains the first bit transmitted while TXDATA[0] the last bit transmitted. When TXDATA[15:0] is octet aligned, TXDATA[15] contains the first bit of the first byte transmitted while TXDATA[0] contains the last bit of the second byte transmitted. TXDATA[15:0] is frequency locked to TXDCK with unspecified static phase

			offset.
TXDSC_P/N	I	DCML	**Transmit Deskew Channel.** The Transmit Deskew Channel (TXDSC) provides reference data to enable skew measurements of the Transmit data bus (TXDATA[15:0]). TXDSC is a 2.488 Gb/s or 2.689 Gb/s stream. TXDSC contains reference frames consisting of 4 framing bytes, 4 bytes of expansion header and 16 sets of 8-byte samples of each signal recovered from the Transmit data bus (TXDATA[15:0]). Samples are taken from the Transmit data bus in a round-robin fashion, starting with TXDATA[15] and ending with TXDATA[0]. TXDSC is frequency locked to TXDCK with unspecified static phase offset.

TXDCK _P/N	I	DCML	**Transmit Data Clock.** The Transmit Data Clock (TXDCK) signal provides timing reference for the Transmit data path signals (TXDATA, TXDSC). TXDCK is nominally a 50% duty cycle clock with a frequency that is one-quarter of the data bit rate of TXDATA and TXDSC. TXDCK is frequency locked to TXCKSRC, TXDSC, and TXDATA. Static phase offset between TXDCK and TXDATA, TXDSC is unspecified. This clock is not used in the Kodiak transponder, but is properly terminated.
TXREFCK_P/N	I	Diff LVPECL	**Transmit Reference Clock.** (TXREFCK) signal is a low jitter input reference at either 1/64 or 1/16 of the optical transmit rate. Normally TXREFCK is used as the reference for the internal clock frequency synthesizer used to generate the 39.813 GHz transmit bit rate clock. Internal to the transponder the frequency of TXREFCK (i.e. the 1/64 rate of 622 MHz, or the 1/16 rate of 2.488 GHz) is selected by the I^2C command TxREFSEL. The incoming signals TXDATA, and TXDSC should be frequency locked to TXREFCK. Static phase offset between TXDCK, TXDSC and TXDATA is unspecified. Selecting between this local reference source TXREFCK or the recovered line clock as the source for the transmitter reference clock is done via either the I^2C command, TxLINETIMESEL, as well as the hardwired pin TXCKSEL. See the I^2C command section for further detail.
TXCKSRC_P/N	O	DCML	**Transmit Clock Source**. The Transmit Clock Source (TXCKSRC) signal from the transponder provides timing reference for the Transmit data path signals (TXDATA, TXDSC, TXDCK). TXCKSRC is nominally a 50% duty cycle clock with a frequency that is one-quarter of the data bit rate of TXDATA and TXDSC. TXCKSRC is derived from the master transmit bit rate clock in the CMU which is in turn derived from either the local input reference TXREFCK or recovered timing from the receive chain. (See description of TXREFCK above)
TXMONCK	O		**Transmit Monitor Clock.** Transmit Monitor Clock provides a single ended clock that can be used to monitor the transmit clock on the mux. For the Kodiak transponder TXMONK is at 1/16 of the transmit bit rate, i.e. 2.488 GHz. See Table 13 for electrical details. This clock signal can be turned on or off using the I^2C command TxMUTEMCLK. The default state for TxMUTEMCLK has TXMONK turned off. (See the supplier reserved command section of Appendix A).
RXMONCK	O		**Receive Monitor Clock.** Transmit Monitor Clock provides a single ended clock that can be used to monitor the receive clock on the demux. This clock is turned off during normal operation and startup. (NOT SUPPORTED)

Notes:

1. For OC-768 / STM-256, bit 15 is the MSB and bit 0 is the LSB. The MSB is transmitted first onto the fiber. P/N denotes the positive and negative sides of the differential signal.

Table 3 Dedicated Alarms and Controls

Name	I/O	Type	Description
MOD_RESET	I	LVTTL	**Transponder Reset.** Active on Low. "0" = reset transponder, "1" = normal operation. Resets all transponder components including CMU, CDR, and all bus registers. [10KOhm pull-up] . To trigger a reset hold the reset state for at least 100ms. After release of reset the transponder I^2C interface will be functional within 20ms and the SFI-5 interfaces will be fully functional within 500ms. The transmit optics will be enabled when their TEC controlled temperatures reach specified operating temperature of around 30C. Depending on the starting temperature this could take from 1-2 seconds for a start close to the operating point, to 30 seconds for a start temperature around 70C.
REG_RESET	I	LVTTL	**Register Reset.** Active on Low. "0" = resets all bus control registers, "1" = normal operation. This resets control registers and will only affect the I2C interface. The signal path of the transponder continues to operate normally. [10K Ohm pull-up]. To trigger a reset hold the reset state for at least 100ms. The I^2C interface is available 1ms after the reset is released.
LS_ENABLE	I	LVTTL	**Enable Laser**. Active on Low. "0" = laser enabled (normal operation), "1" = laser disabled. [10KOhm pull-up] Note that this operating state can also be changed via the I^2C command LS_ENABLE which also has as its default condition a "0" for laser enabled. The Pin and I^2C commands are 'or'd so that changing either one to 'high' will disable the laser. See the state table in the I^2C section *A.3.1.1.1 Set TX Command Register.* The laser is fully turned on 10ms after the LS_ENABLE is turned on.
LOS	O	LVTTL	**Loss of Signal Alarm.** Active on Low. "0" = Alarm, "1" = normal operation. Indicates that there is no incoming optical signal. Note that this alarm represents the instantaneous state of the input signal - i.e. it is not latched after being triggered. LOS is detected in hardware and is asynchronous with respect to the micro-controller. The signal is low pass filtered with a 2.5 μsec time constant, so drop-outs lasting less than 2 μs are ignored. Loss of signal is detected within 50 μs. LOS is triggered when the input optical signal drops below -10.5 dBm and will then turn off when the signal rises above -9.5dBm.
STAT_INT	O	LVTTL	**Status Interrupt.** Active on Low. "0" = Alarm, "1" = normal operation. Indicates one of the internal alarms is triggered. This signal pin has an active pull-up. The internal alarms are read over the I^2C bus. Note that this alarm represents the instantaneous state of the alarms in the transponder - i.e. it is not latched after being triggered.
CFG_ALM	O	LVTTL	**Configurable Alarm**. Active on Low. "0" = Alarm, "1" = normal operation. An I^2C configurable alarm output. Typically used for an alarm or status indicator where 'real time' indication of a change is desired. (See I^2C Alarm Table for further detail on configuring this alarm). [This signal is open collector]
TXCKSEL	I	LVTTL	**Transmit Clock Select.** Selects whether the transmit clock reference is taken from a local reference or from the recovered clock of the incoming optical data. "0" = select recovered timing, "1" = select local reference, TXREFCK. [10KOhm pull-up] Note that this operating state can also be changed via the I^2C command TxLINETIMSEL which also has as its default condition a "1" for local timing. The Pin and I^2C commands are 'or'd so that switching to recovered timing requires both pin and I^2C command to be in the '0' state. See the state table in the I^2C section *A.3.1.1.1 Set TX Command Register*

Table 4: Alarm Response Time

Alarm	Response Time (Activation)			Response Time (Deactivation)		
	Minimum	Typical	Maximum	Minimum	Typical	Maximum
CFG_ALM			10 ms			10 ms
LOS			50 µs			50 µs
RXS (Note 1)	10 µs	100 µs	10 ms	500 µs	2 ms	10 ms

Note 1: Under a fault condition of constant light input with no data modulation, the RXS error signal may toggle between the 'lock-error' state and the 'no-lock-error' state.

Table 5 I^2C Interface Bus

The transponder adheres to the 40G MSA specification for the I^2C interface. The physical interface bus is summarized in the table below with further detail given in section 2.1 of Appendix A.

Name	I/O	Type	Description
I2C_SDA	I/O	Open Collector	**I^2C Data line**
I2C_SCL	I	Open Collector	**I^2C Clock line**
I2C_ADDR[2:0]	I	LVTTL	**I^2C Address [2:0]** Transponder 3 bit address. [1KOhm pull-down]

The hardware layer of the interface adheres to the Philips ® Semiconductor definition of the I^2C bus. The components used on the transponder are registered with Philips. The firmware interface provides a means of transferring data and control information between the host system and the transponder.

The transponder I^2C address is made up of a fixed part and a configurable part. The configurable part is three bits long, and is set by the I2C_ADDR[2:0] pins on the 300-pin MegArray connector.

I^2C Address (7 bit)	Device
0x1000xxxR	Transponder

Note: xxx = user selectable 3 bit transponder address and R = Read/Write bit.

I^2C Protocol Interface

The transponder adheres to the 40G MSA specification for the I^2C interface protocol. Additional features specific to the Big Bear transponder may also be incorporated. All protocol details are provided in Appendix A.

Table 6: Power & Ground Signals

Name	I/O	*Type*	Description
3.3V Digital	I	Supply	Power supply, +3.3V Digital
3.3V Analog	I	Supply	Power supply, +3.3V Analog
APS Digital	I	Supply	Adaptable Power Supply, Digital
-5.2VDigital	I	Supply	Power supply, -5.2V Digital
-5.2VAnalog	I	Supply	Power supply, -5.2V Analog
5.0VAnalog	I	Supply	Power supply, 5.0V Analog
DigitalGND	I	Ground	Digital ground
AnalogGND	I	Ground	Analog ground
FM_GND	I	Ground	Transponder Case
APS Sense	O	Analog Signal	Zero ohm sense connection to the 1.8V internal supply of the transponder. Placeholder pin for the sense line of an adjustable power supply feature.
APS_Set	O	Analog Signal	Used to set the value of the APS voltage between 0.9V and 1.8V. Kodiak transponder currently operates with an APS voltage of 1.8V. The APS circuits are shown below in Figure 4. Tying APS Set to ground sets the operating state to 1.8V.
NuC	NuC		No user Connection. Must remain open circuits.

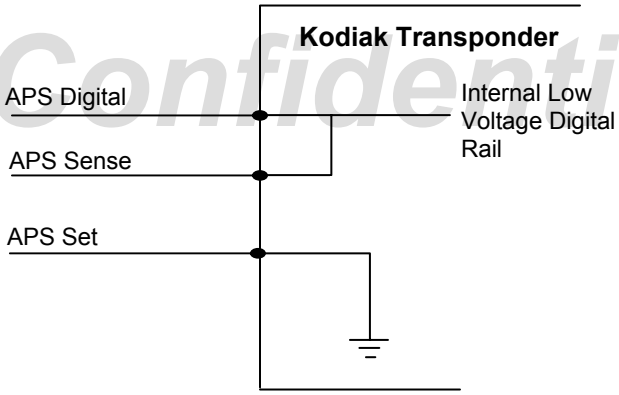


Figure 4 Adaptable Power Supply (APS) Lines

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 7 Absolute Maximum Ratings

Rating	*Symbol*	*Min*	*Max*	*Units*
Storage Case Temperature	T_{stg}	–40	+85	°C
Receive Optical Input Power P_{IN}	P_{MAX}		+6	dBm
Minimum Fiber Bend Radius		30		mm
+3.3V Supplies (Note 1)		-0.3	+3.6	V
+1.8V Supplies (Note 1)		-0.3	+2.0	V
+5.0V Supplies		-0.3	+6.0	V
-5.2V Supplies		-5.5	+0.3	V
LV-TTL Input Voltage		-0.2	3.3VDigital + 0.2	V
LV-TTL Output Voltage		-0.2	3.3VDigital + 0.2	V
CML Output Source Current			20	mA
Static Discharge Voltage (Note 2)	ESD		25KV Air Discharge	V
Relative Humidity (non-condensing)	RH	15	85	%

Note 1: This is the maximum potential difference allowed in order to avoid device degradation during product use conditions.
Note 2: Per IEC 801.2 (Class 1A product)

Recommended Operating Conditions

Minimum and maximum values specified over operating case temperature range at 50% duty cycle data signal. Typical values are measured at room temperature unless otherwise noted. Note that the transponder contains internal protection circuitry which permits any power-up sequence.

Table 8 Standard Operating Conditions

Parameter	*Name*	*Conditions*	*Min*	*Typical*	*Max*	*Units*
Operating Case Temperature	T_C	Notes 1	0		70	°C
Transponder Power Consumption	P_{DIS}			26	32	W
+3.3V Power Supply Voltage (Digital)	3.3VDigital		3.135	3.3	3.465	V
+3.3V Power Supply Voltage (Analog)	3.3VAnalog		3.135	3.3	3.465	V
+1.8V Power Supply Voltage (Digital)	APS Digital		1.71	1.8	1.89	V
-5.2V Power Supply Voltage (Analog)	-5.2VAnalog		-5.45	-5.2	-4.95	V
-5.2V Power Supply Voltage (Digital)	-5.2VDigital		-5.45	-5.2	-4.95	V
+5.0V Power Supply Voltage (Analog)	+5.0VAnalog		4.75	5.0	5.25	V
+3.3V Power Supply Current (Digital)	3.3VDigital	Note 2		2300	2700	mA
+3.3V Power Supply Current (Analog)	3.3VAnalog			2500	3000	mA
+1.8V Power Supply Current (Digital)	APS Digital			700	1000	mA
-5.2V Power Supply Current (Analog)	-5.2VAnalog			1400	2000	mA
-5.2V Power Supply Current (Digital)	-5.2VDigital			1400	2000	mA
+5.0V Power Supply Current (Analog)	5.0VAnalog			0	100	mA
Ripple and Noise		1Hz to 20MHz			1%	mVpp

Notes: 1. See Figure 5 for location of temperature measurement points. Detailed thermal operating data to be supplied upon request.
2. The maximum transient current for the 3.3V Digital is 3500mA during TEC turn-on.

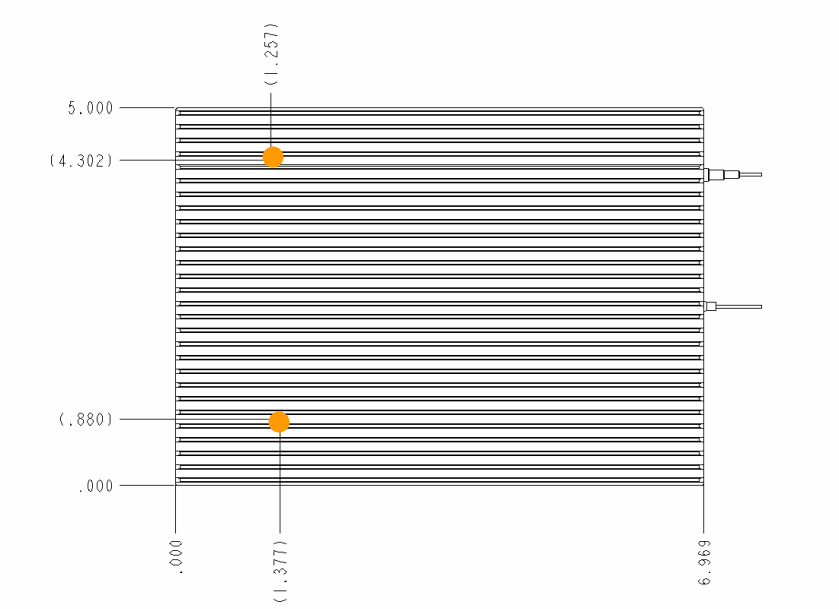


Figure 5: Recommended Temperature Measurement Points

Optical Characteristics

Minimum and maximum values specified over operating case temperature range at 50% duty cycle data signal. Typical values are measured at room temperature unless otherwise noted. All values are stated for end-of-life.

Table 9: 40G Short Reach Optical Transponder Characteristics (SR1: 5dB budget, ~2km reach, Note 1)

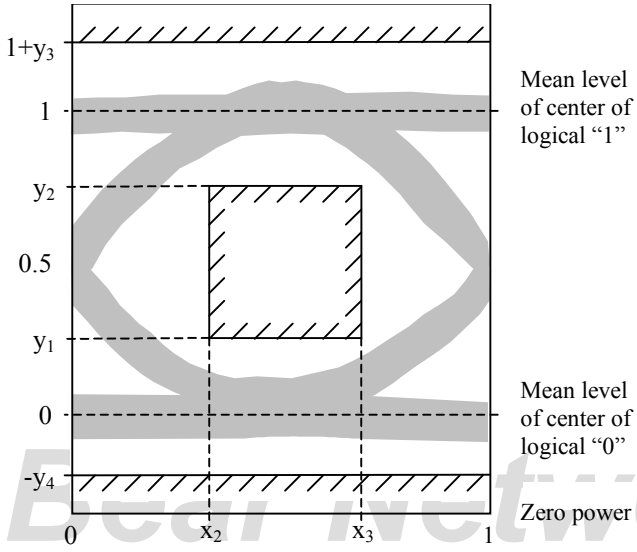
Parameter	*Symbol*	*Conditions*	*Min*	*Typical*	*Max*	*Units*
Transmitter						
Operating Wavelength	λ_C		1530	1555	1565	nm
Output Power	P_O		0		+3	dBm
Extinction Ratio	ER		8.2			dB
Spectral Width	$\Delta\lambda_{RMS}$	@ -20dB			1	nm
Side Mode Suppression Ratio	SMSR		35			dB
Receiver						
Nominal Center Wavelength	λ_{NOM}		1290		1570	nm
Stressed Sensitivity	P_{IN}	@10^{-12} BER Note 2	-5			dBm
Overload	P_{OL}		+3			dBm
Optical Return Loss	RL_{RX}		27			dB
Optical Path						
Optical Link Loss	OL		0		4	dB
Path Penalty/System Margin	M	Note 2	0		1	dB
Dispersion	D		-40		40	ps/nm
Polarization Mode Dispersion	DGD				7.5	ps
System Optical Return Loss			24			dB

Notes:

1. Aligned with the ITU G.693 specification for NRZ 40G 2km applications (VSR2000-3R2, VSR2000-3R3, VSR2000-3R5)
2. Stressed receiver sensitivity includes worst-case ER penalty, transmitter patterning allowance, and other receiver impairments. This corresponds to a back-to-back measurement without fiber and without path penalty, per section 6.4 of ITU-T G.693.

Optical Transmit Eye Pattern Mask

The optical eye mask satisfies the specification provided in ITU-T Recommendation G.693, “Optical interfaces for intra-office systems”, October 2001. The parameters specifying the mask of the transmitter eye diagram are shown in Figure 6.



	NRZ 40G
x_3-x_2	0.2
y_1	0.25
y_2	0.75
y_3	0.25
y_4	0.25

Figure 6: Mask of the eye diagram for the optical transmit signal

Note - x_2 and x_3 of the rectangular eye mask need not be equidistant with respect to the vertical axes at 0 UI and 1 UI.

Electrical Characteristics

Table 10 LV-TTL Input and Output Characteristics

Parameter	*Symbol*	*Conditions*	*Min*	*Typical*	*Max*	*Units*
LV-TTL Input DC Characteristics						
Input High Voltage	V_{IH}	TTL V_{CC1}= Max	2.0		3.6	V
Input Low Voltage	V_{IL}	TTL V_{CC1}=Min	0		0.8	V
Input High Current	I_{IH}	V_{IN}=2.4V			50	µA
Input Low Current	I_{IL}	V_{IN} =0.5V	-50			µA
LV-TTL Output DC Characteristics						
Output High Voltage	V_{OH}	V_{CC2}=Min, I_{OH}=-8mA	2.4			V
Output Low Voltage	V_{OL}	V_{CC2}=Min I_{OL}= 1mA			0.4	V

Table 11 CML Input and Output Characteristics

Parameter	*Symbol*	*Conditions*	*Min*	*Typical*	*Max*	*Units*
CML Differential DC-Coupled Input Characteristics Applies to TXDATA[15:0], TXDCK, and TXDSC						
Termination Voltage	V_{tt}	p-p value (Note 1)	1.1	1.2	1.3	V
Input Sensitivity	VR_{Sense}	p-p voltage	175			mV
Bias Voltage Source Impedance	ZV_{tt}	(Note 2)			30	Ω
Rise/Fall Time	$T_{Rise/Fall}$	20-80%. Measured differentially into a 100 ohm load			0.36	UI
Differential Input Voltage Swing	VR_{IN}	p-p voltage (Note 3)	0.175		1.15	V
Common Mode Voltage	VR_{CM}	(Note 4)	0.7		Vtt	V
Differential Input Impedance	Z_{InDiff}	(Note 5), *Figure 7*	75		125	Ω
Differential Return Loss	L_{DR}	(Note 6)	10			dB
CML Differential AC-Coupled with DC Bias Output Characteristics Applies to RXDATA[15:0], RXDCK, and RXDSC						
Driver Rise/Fall Time	TD_{RF}	20% - 80% into 100 ohm load	50			ps
Differential Output Voltage Swing	V_{DO-CML}	p-p voltage	0.6	0.8	1.0	V
Single-ended Output Impedance	Z_{SE}	≥ 10KHz, (Note 7)	37.5		62.5	Ω
Differential Output Impedance	Z_D	≥ 10KHz, (Note 8)	75		125	Ω
Single-ended Return Loss	R_{HS}	(Note 9)	7.5			dB
Differential Return Loss	RL_{Diff}	(Note 10)	7.5			dB

CML Differential DC-Coupled Output Characteristics Applies to TXCKSRC						
Output Common Mode Voltage	V_{CM}	(Note 11)	0.72V		1.23V	V
Driver Rise/Fall Time	TD_{RF}	Refer to eye mask definition in *Table 18*				ps
Differential Output Voltage Swing	V_{DO-CML}	p-p voltage	0.6	0.8	1.0	V
Short Circuit Current	I_{Short}	To any voltage between 1.45V & -0.25, power on or off	-50		50	mA
Single-ended Output Impedance	Z_{SE}	At DC	37.5		62.5	Ω
Differential Output Impedance	Z_D	At DC	75		125	Ω
Single-ended Return Loss	R_{HS}	(Note 9)	7.5			dB
Differential Return Loss	RL_{Diff}	(Note 10)	7.5			dB

Notes:

1. Specified for both AC and DC coupling applications
2. From DC to .75*baud rate if DC blocking capacitors are not present. From 500Mhz to .75*baud rate if DC blocking capacitors are present.
3. Peak-Peak voltage. Zrterm=62.5 ohms.
4. (Vhigh + Vlow) / 2
5. At DC. Parameter is unspecified if DC blocking capacitors are present.
6. From 0.004*baud rate to 0.75*baud rate relative to 100 ohms.
7. At DC the single ended output impedance is 10K ohms.
8. At DC the differential output impedance is 20K ohms.
9. From 0.004*baud rate -0.75*baud rate. Relative to 50 ohms.
10. From 0.004*baud rate -0.75*baud rate. Relative to 100 ohms.
11. (Vhigh + Vlow) / 2. When using a load of *Figure 7* with 1.05 < Vtt < 1.35 Volts, 37.5 < rterm< 62.5 ohms, 0< Zvtt < 30 ohms. Ground in Figure 7 is the same as driver ground. Vtt values take into account the assumption of up to ± 50mV ground shift between transmit and receive. Parameter is unspecified if DC blocking capacitors are present.

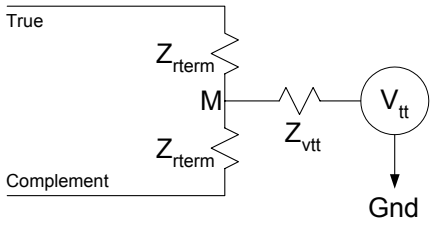


Figure 7 Termination and Signaling

Table 12: Input Reference Clock Characteristics

Parameter	*Symbol*	*Conditions*	*Min*	*Typical*	*Max*	*Units*
Differential Input Impedance	$Z_{In\ Diff}$	AC Coupled	90	100	110	Ω
Differential Input Voltage	$V_{In\ Diff}$	Peak - peak	400	800	1800	mV
Nominal VCO Reference Center Frequency	TXREFCK RXREFCK			622.08		MHz
Nominal VCO Reference Center Frequency	TXREFCK RXREFCK	(NOT SUPPORTED see Note 1)		2.488		GHz
Reference Clock Frequency Tolerance	$TXREFCK_{Tol}$ $RXREFCK_{Tol}$	± 20ppm required to meet SONET/SDH output requirements	-30		30	ppm
Reference Clock Jitter		12.8 KHz to 20 KHz			2	ps rms
Reference Clock Input Duty Cycle	$TXREFCK_{DC}$ $RXREFCK_{DC}$		45		55	%
Reference Clock Rise & Fall Times	T_R, T_F	Note 2			100 ps	

Notes:

1. Current versions of Kodiak transponder require TXREFCK and RXREFCK to be 1/64 of the optical transmit data rate.
2. An input reference clock consisting of a sine wave can also be used with a very minor increase in low frequency jitter.

Table 13 TXMONK Specifications

Parameter	*Conditions*	*Min*	*Typical*	*Max*	*Units*
Output Voltage	Single Ended Peak - Peak, AC coupled		400		mV
Nominal Frequency			2.488	2.689	GHz
Duty Cycle		45		55	%
Rise & Fall Times				100 ps	

Table 14 I²C Electrical Characteristics (DC)

Parameter	Symbol	Conditions	Min	Typical	Max	Units
High Level Input Voltage	V_{IH}		1.9		5.5	V
Low Level Input Voltage	V_{IL}		-0.5		1.65	V
Hysteresis	V_{HYS}		0.28			V
Low Level Output Voltage	V_{OL}				0.4	V
Capacitance for each I/O pin	C				10	pF

Table 15 I²C Electrical Characteristics (AC)

Parameter	Symbol	Conditions	Min	Typical	Max	Units
SCL Frequency	F_{SCL}		0		400	kHz
Hold Time (repeated) START	$t_{hd,sta}$	>100KHz	0.6		---	µS
Low Period of SCL	t_{Low}	>100KHz	1.3		---	µS
High Period of SCL	t_{High}	>100KHz	0.6		---	µS
Rise Time of SCL, SDA	t_{Rise}		---		300	nS
Fall Time of SCL, SDA	t_{Fall}		---		250	nS

The interface operates in FAST-mode with a data transfer rate of 400Kbps, or it can operate in 100Kbps mode. The design uses level translators to ensure proper operation with any host system that uses a 3.3V or greater supply voltage. As shown in Figure 8 below, the line card needs to provide pull-up resistors for the SCL and SDA lines. The number of I²C devices in the system determines the value of the pull-up resistors Rp.

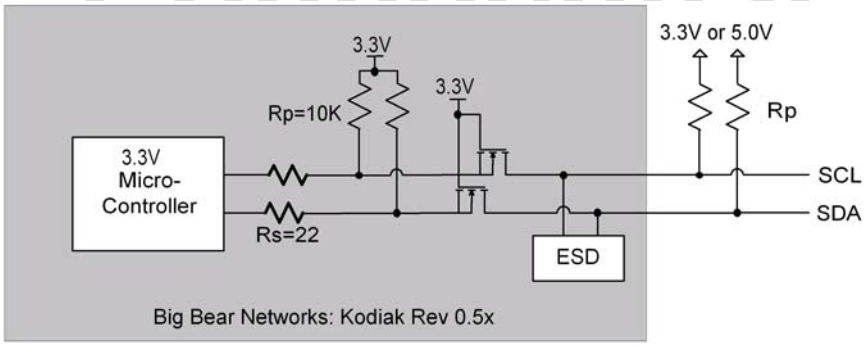


Figure 8 I²C Interface

I²C Command Latency

Following a Hardware Reset

There is a 20 ms delay from the rising edge of MOD_RESET to the time the transponder is ready to receive a command.

Command-to-Command

The maximum command execution latency is 125 microseconds. This specifies the time from when the last command byte has transferred to the transponder to when the transponder has executed that command and the results are available. This does not apply to Save or Restore type commands or any other command that must read or write the flash. If the system is polled before the command has finished executing it will return the response "Still Processing" (See Appendix Section A.2.6 for further detail on the status byte).

SFI-5 Eye Mask & Jitter Specifications

The eye mask defines the horizontal (jitter) and vertical (signal amplitude) characteristics for the SFI-5 data and clock signals. The eye masks are defined for the transponder inputs (TXDATA) and the transponder outputs (RXDATA).

The following eye mask and jitter specifications follow the OIF-SXI5-01.0 (Oct 2002) specification format. Note that the correspondence between the OIF and Kodiak Transponder parameters are shown below in *Table 16 Transport Path Parameter Correspondence.*

Table 16 Transport Path Parameter Correspondence

Transport Path	Kodiak Transponder	OIF-SXI5-01.0 (OCT 2002)
Framer/FEC to SERDES	TXDATA (SFI-5 input to Transponder)	Receive Eye Mask: Reference Point 'D'
SERDES to Framer/FEC	RXDATA (SFI-5 output from Transponder)	Transmit Eye Mask: Reference Point 'A'

The rationale for the correspondence is shown in the following figures. Figure 9, which is taken from the OIF specification, shows the system reference points for the eye mask and jitter specifications of the OIF specification. Normally the timing for TXDATA flow is taken from the local PLL in the CMU of the Transponder. Therefore using the OIF interface definition shown in Figure 10 the TXDATA eye diagram and jitter correspond to reference point 'D'.

In the case of RXDATA the timing is also regenerated in the CDR of the transponder so the relevant reference point is 'A'.

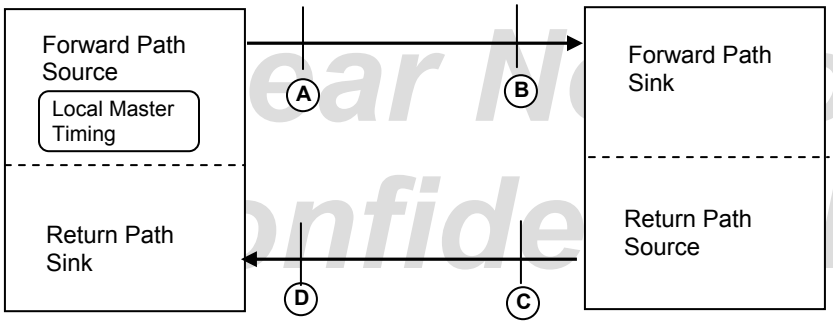


Figure 9 Eye Mask and Jitter Reference Diagram (see OIF-SXI5-01.0 Fig 6)

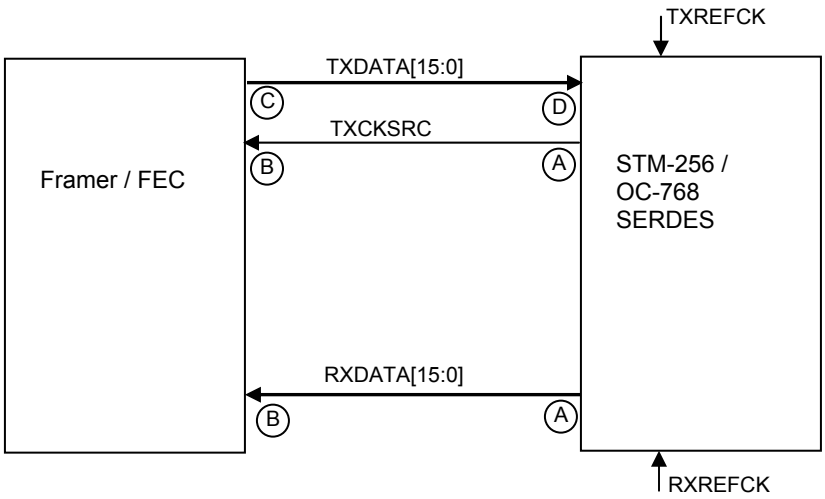


Figure 10 Schematic Diagram of Framer / FEC Processor to SERDES Transponder Interface (see OIF-SFI5-01.0 Fig5.1)

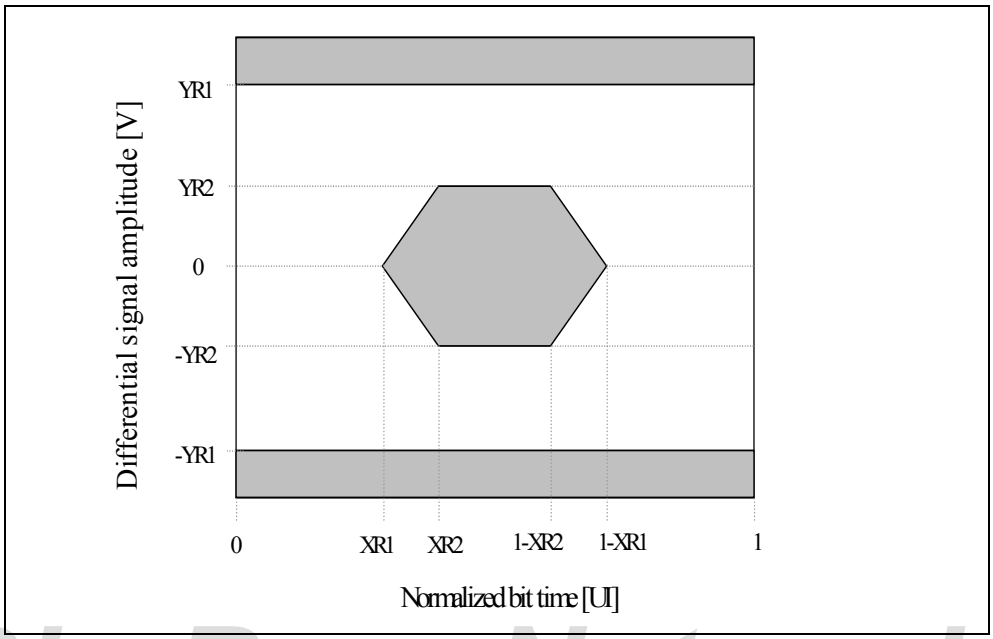


Figure 11 SFI-5 TXData Eye Mask
(Eye at the TXDATA Input)

Table 17 SFI-5 TxData Eye Mask Specifications

Data / Clock	*XR1 (UI)*	*XR2 (UI)*	*YR1 (V)*	*YR2 (V)*	*DJ [pp UI]*	*Total Jitter J_{Tot} [pp UI]*
TXDATA (Notes 1,2,3)	0.33	0.42	0.5	0.0875	0.35	0.65
TXDCK	0.27	0.39	0.5	0.0875	0.24	0.54

Notes:

1. TXDATA Eye Mask Specifications taken from OIF-SXI5-01.0 (Oct 2002) Receive Eye Mask Specifications (Table 5) using reference point 'D'
2. TXDATA received eye mask at receiver pin measured with a signal from a 100 Ohm source that has more than 20dB return loss at a frequency of 1.6 * baud rate.
3. The horizontal limit specified in the eye mask shown in *Figure 11* represents the total jitter seen at the receiver input (both random jitter and deterministic jitter).

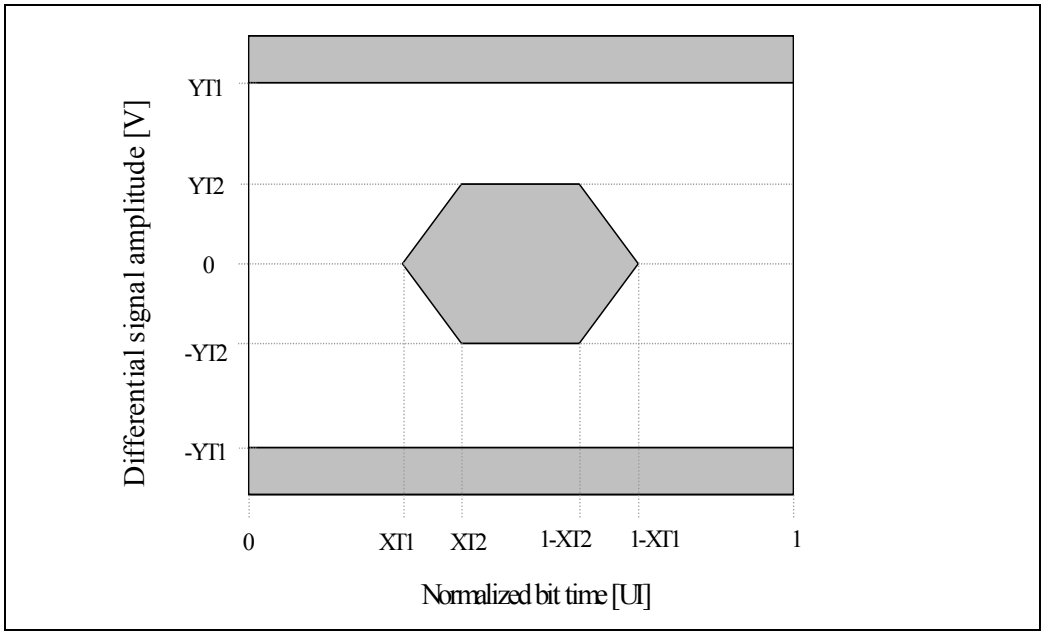


Figure 12 SFI-5 RXData Eye Mask
(Eye at the RXDATA output)

Table 18 SFI-5 RXData Eye Mask Specifications

Data / Clock	*XT1 (UI)*	*XT2 (UI)*	*YT1 (V)*	*YT2 (V)*	*DJ [pp UI]*	*Total Jitter J_{Tot} [pp UI]*
RXDATA (Notes 1,2,3)	0.175	0.45	0.50	0.25	0.17	0.35
RXDCK	0.15	0.45	0.50	0.25	0.12	0.30
TXCKSRC	0.15	0.45	0.50	0.25	0.12	0.30

Notes:

1. RXDATA Eye Mask Specifications taken from OIF-SXI5-01.0 (Oct 2002) Transmit Eye Mask Specifications (Table 4) using reference point 'A'.
2. RXDATA eye mask at driver pin measured into a 100 Ohm load having more than 20dB return loss at a frequency of 1.6 * baud rate.
3. The horizontal limit specified in the eye mask shown in *Figure 12* represents the total jitter seen at the driver output (both random jitter and deterministic jitter).

Table 19 SFI-5 Jitter Specifications

Parameter	*TYPE*	*RXDATA& RXDSC* (Note 1)	*TXDATA & TXDSC* (Note 2)	*UNITS*
Skew	Data	2.0	5.0	UI peak
Correlated Wander	All	4.5	10.0	UI peak to peak
Uncorrelated Wander	All	0.60	0.65	UI peak to peak
Total Wander	All	5.1	10.65	UI peak to peak
Relative Wander	All	1.2	1.3	UI peak to peak
Skew + (Relative Wander)/2	Data	2.6	5.65	UI peak

Notes:

1. RXDATA Jitter Specifications taken from OIF-SXI5-01.0 (Oct 2002) (Table 3) using reference point 'A'.
2. TXDATA Jitter Specifications taken from OIF-SXI5-01.0 (Oct 2002) (Table 3) using reference point 'D'

Jitter Characteristic

It is the intention that the Kodiak Transponder be compatible with future (in-development) OC-768 / STM-256 ANSI and ITU jitter specifications. The specifications given herein are derived from G.693 and the ongoing work within the ITU on the specification of G.8251 (formerly G.otnjit) for OTU3 interfaces with ODU3 Clock (ODC) ODCb requirements.

Jitter Generation

Jitter generation is specified to comply with G.8251 and G.693 requirements. The first of these essentially limits the amount of random jitter generated by the transponder. The jitter generation shall not exceed the values given in *Table 20 G.8251 OTU3 Jitter Generation Limits* for a 60-second measurement interval using a jitter filter with the indicated bandwidths. Specifically, the jitter band-pass filter possesses 0dB mid-band gain, a 20dB/decade roll-off below F0 and a 60-dB/decade roll-off above F1.

Table 20 G.8251 OTU3 Jitter Generation Limits

Measurement	*F0 (kHz)*	*F1 (MHz)*	*J (UI-p-p)*[1]
Wide-Band	20	320	1.2
High-Band	16,000	320	0.1

Note 1. The unit of 1 UI is defined to be 23.25ps for 43 Gb/s operation, and should be scaled for 39.8131 Gb/s use. See G.8251, Rev. 4.0, Table A.2.

The second set of requirements limits the total high-frequency (i.e. untracked) jitter, including deterministic and random sources. These requirements are still in the process of being defined. The Kodiak Transponder will be compatible with applicable industry standards, G.693.

Jitter Tolerance

The jitter tolerance meets or exceeds the requirements for OTU3 interfaces, the details of which are provided below. Values taken from G.8251 Table 4.

Table 21 G.8251 OTU3 Interface Jitter Tolerance

F1 (kHz)	*F2 (kHz)*	*F3 (kHz)*	*F4 (kHz)*	*F5 (MHz)*
8	20	400	16,000	320

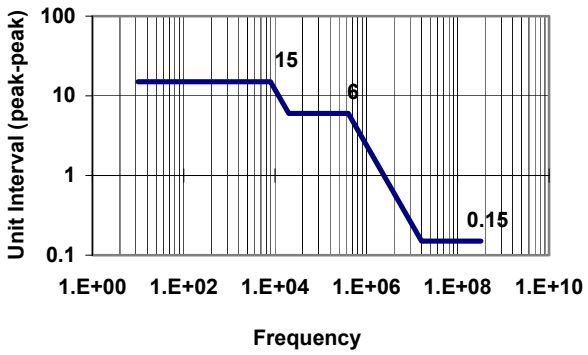


Figure 13 G.8251 OTU3 Interface Jitter Tolerance Mask (UI peak-peak)

Jitter Transfer

The Jitter transfer will be less than 0.1 dB peaking up to 16 KHz corresponding to ODCb type systems. *Table 22 Jitter Transfer* below shows the ODU3 ODCb break frequencies.

Table 22 Jitter Transfer

OTN Interface and Equipment Type	***F_L (Hz)***	***F_C (KHz)***	***F_H (KHz)***	***P (dB)***
ODU3 / ODCb	160	16	1600	0.1

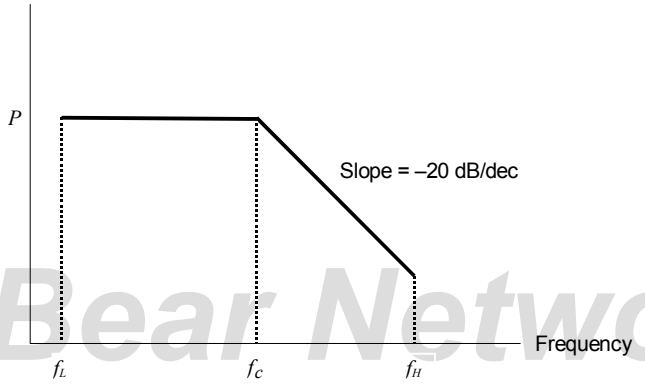


Figure 14 Jitter Transfer (G.8251 ODCb)

Connector Pin-out Diagram

Kodiak Transponder 300-pin MegArray receptacle connector pin-out.

	K	J	H	G	F	E	D	C	B	A
1	DigitalGND	RXDSCP	DigitalGND	RXDATA12P	DigitalGND	RXDATA8P	DigitalGND	RXDATA4P	DigitalGND	RXDATA0P
2	DigitalGND	RXDSCN	DigitalGND	RXDATA12N	DigitalGND	RXDATA8N	DigitalGND	RXDATA4N	DigitalGND	RXDATA0N
3	FFU	DigitalGND	-5.2VDigital	DigitalGND	FFU	DigitalGND	APS Digital	DigitalGND	3.3VDigital	DigitalGND
4	DigitalGND	RXDCKP	DigitalGND	RXDATA13P	DigitalGND	RXDATA9P	DigitalGND	RXDATA5P	DigitalGND	RXDATA1P
5	DigitalGND	RXDCKN	DigitalGND	RXDATA13N	DigitalGND	RXDATA9N	DigitalGND	RXDATA5N	DigitalGND	RXDATA1N
6	LOS	DigitalGND	-5.2VDigital	DigitalGND	I2C_ADDR_0	DigitalGND	APS Digital	DigitalGND	3.3VDigital	DigitalGND
7	DigitalGND	RXREFCKP	DigitalGND	RXDATA14P	DigitalGND	RXDATA10P	DigitalGND	RXDATA6P	DigitalGND	RXDATA2P
8	DigitalGND	RXREFCKN	DigitalGND	RXDATA14N	DigitalGND	RXDATA10N	DigitalGND	RXDATA6N	DigitalGND	RXDATA2N
9	FFU	DigitalGND	-5.2VDigital	DigitalGND	I2C_ADDR_1	DigitalGND	APS Digital	DigitalGND	3.3VDigital	DigitalGND
10	I2C_SDA	FFU	DigitalGND	RXDATA15P	DigitalGND	RXDATA11P	DigitalGND	RXDATA7P	DigitalGND	RXDATA3P
11	DigitalGND	RXMONCK	DigitalGND	RXDATA15N	DigitalGND	RXDATA11N	DigitalGND	RXDATA7N	DigitalGND	RXDATA3N
12	I2C_SCL	DigitalGND	RXS	DigitalGND	I2C_ADDR_2	DigitalGND	APS Digital	DigitalGND	3.3VDigital	DigitalGND
13	FFU	NUC	NUC	NUC	NUC	NUC	APS SENSE	NUC	NUC	FFU
14	AnalogGND	-5.2VAnalog	AnalogGND	-5.2VAnalog	AnalogGND	3.3 VAnalog	AnalogGND	3.3VAnalog	AnalogGND	5.0VAnalog
15	AnalogGND	-5.2VAnalog	AnalogGND	-5.2VAnalog	AnalogGND	3.3 VAnalog	AnalogGND	3.3VAnalog	AnalogGND	5.0VAnalog
16	AnalogGND	-5.2VAnalog	AnalogGND	-5.2VAnalog	AnalogGND	3.3VAnalog	AnalogGND	3.3VAnalog	AnalogGND	5.0VAnalog
17	FFU	NUC	NUC	NUC	NUC	NUC	APS SET	NUC	NUC	FFU
18	DigitalGND	TXMONCK	FFU	FFU	DigitalGND	FFU	FFU	FFU	FFU	FFU
19	LS_ENABLE	DigitalGND	-5.2VDigital	DigitalGND	CFG_ALM	DigitalGND	APS Digital	DigitalGND	3.3VDigital	DigitalGND
20	DigitalGND	TXDSCP	DigitalGND	TXDATA12P	DigitalGND	TXDATA8P	DigitalGND	TXDATA4P	DigitalGND	TXDATA0P
21	DigitalGND	TXDSCN	DigitalGND	TXDATA12N	DigitalGND	TXDATA8N	DigitalGND	TXDATA4N	DigitalGND	TXDATA0N
22	STAT_INT	DigitalGND	-5.2VDigital	DigitalGND	TXCKSEL	DigitalGND	APS Digital	DigitalGND	3.3VDigital	DigitalGND
23	DigitalGND	TXDCKP	DigitalGND	TXDATA13P	DigitalGND	TXDATA9P	DigitalGND	TXDATA5P	DigitalGND	TXDATA1P
24	DigitalGND	TXDCKN	DigitalGND	TXDATA13N	DigitalGND	TXDATA9N	DigitalGND	TXDATA5N	DigitalGND	TXDATA1N
25	REG_RESET	DigitalGND	-5.2VDigital	DigitalGND	APS Digital	DigitalGND	APS Digital	DigitalGND	3.3VDigital	DigitalGND
26	DigitalGND	TXCKSRCP	DigitalGND	TXDATA14P	DigitalGND	TXDATA10P	DigitalGND	TXDATA6P	DigitalGND	TXDATA2P
27	DigitalGND	TXCKSRCN	DigitalGND	TXDATA14N	DigitalGND	TXDATA10N	DigitalGND	TXDATA6N	DigitalGND	TXDATA2N
28	MOD_RESET	DigitalGND	-5.2VDigital	DigitalGND	APS Digital	DigitalGND	APS Digital	DigitalGND	3.3VDigital	DigitalGND
29	DigitalGND	TXREFCKP	DigitalGND	TXDATA15P	DigitalGND	TXDATA11P	DigitalGND	TXDATA7P	DigitalGND	TXDATA3P
30	DigitalGND	TXREFCKN	DigitalGND	TXDATA15N	DigitalGND	TXDATA11N	DigitalGND	TXDATA7N	DigitalGND	TXDATA3N

Figure 15 Connector Pin-Out Diagram

Differential CML Signals
Differential AC Signals
Power
Ground
Control Signals
For Future Use

Pin Assignment Table

To Be Inserted

Package Outline Diagram

Table 23 Mechanical Dimensions

Parameter	*Value (inches)*	*Value (Metric)*
Length	6.969 "	177 mm
Width	5.0 "	127 mm
Height (without heatsink)	0.65 " (Note 1)	16.5 mm
Pigtail length	39.4 " ± 4"	100 ± 10 cm
Type of electrical interface	300 pin Berg MegArray	
Type of optical interface	Device Option (see ordering info)	

NOTES
1. Heatsinks can be incorporated - contact Big Bear for further details.

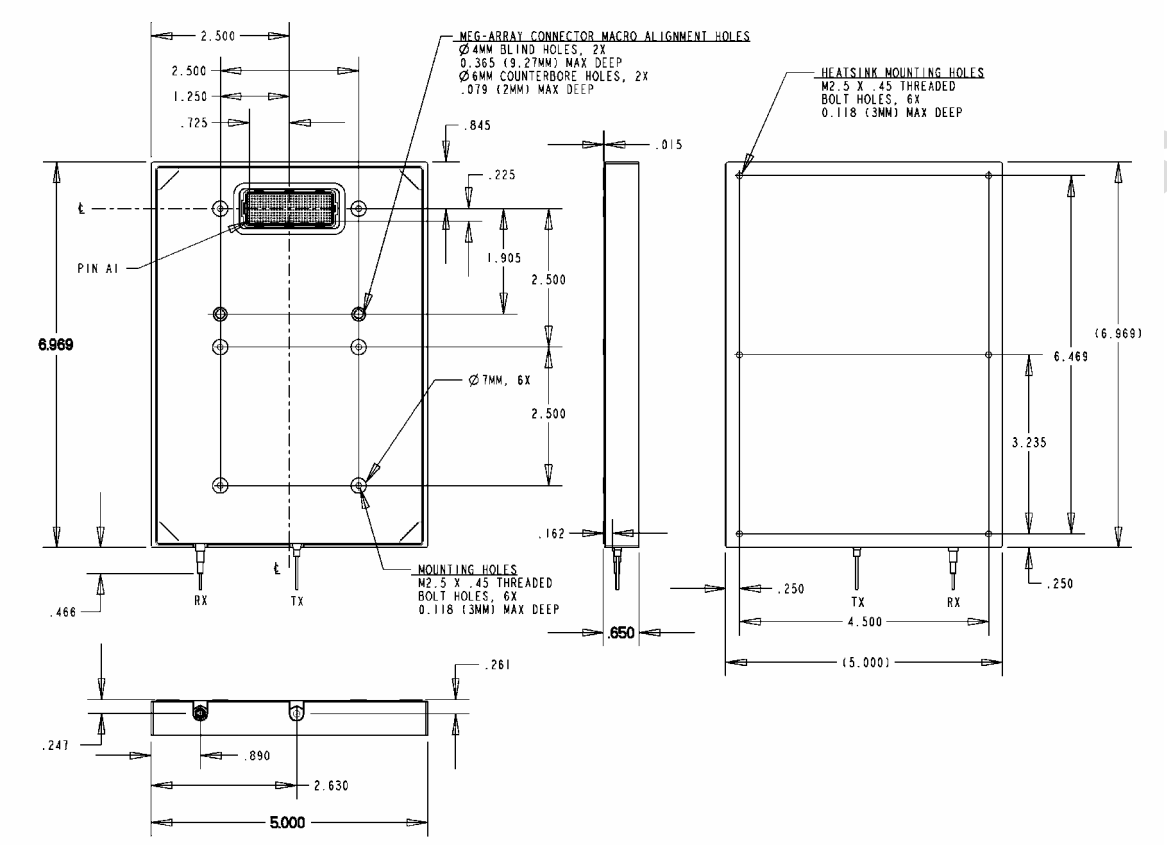


Figure 16 Transponder Mechanical Drawing (Bottom View and Side View)

NOTE: When mounting the transponder the screws should be tightened using a torque screw-driver (2 inch-lb).

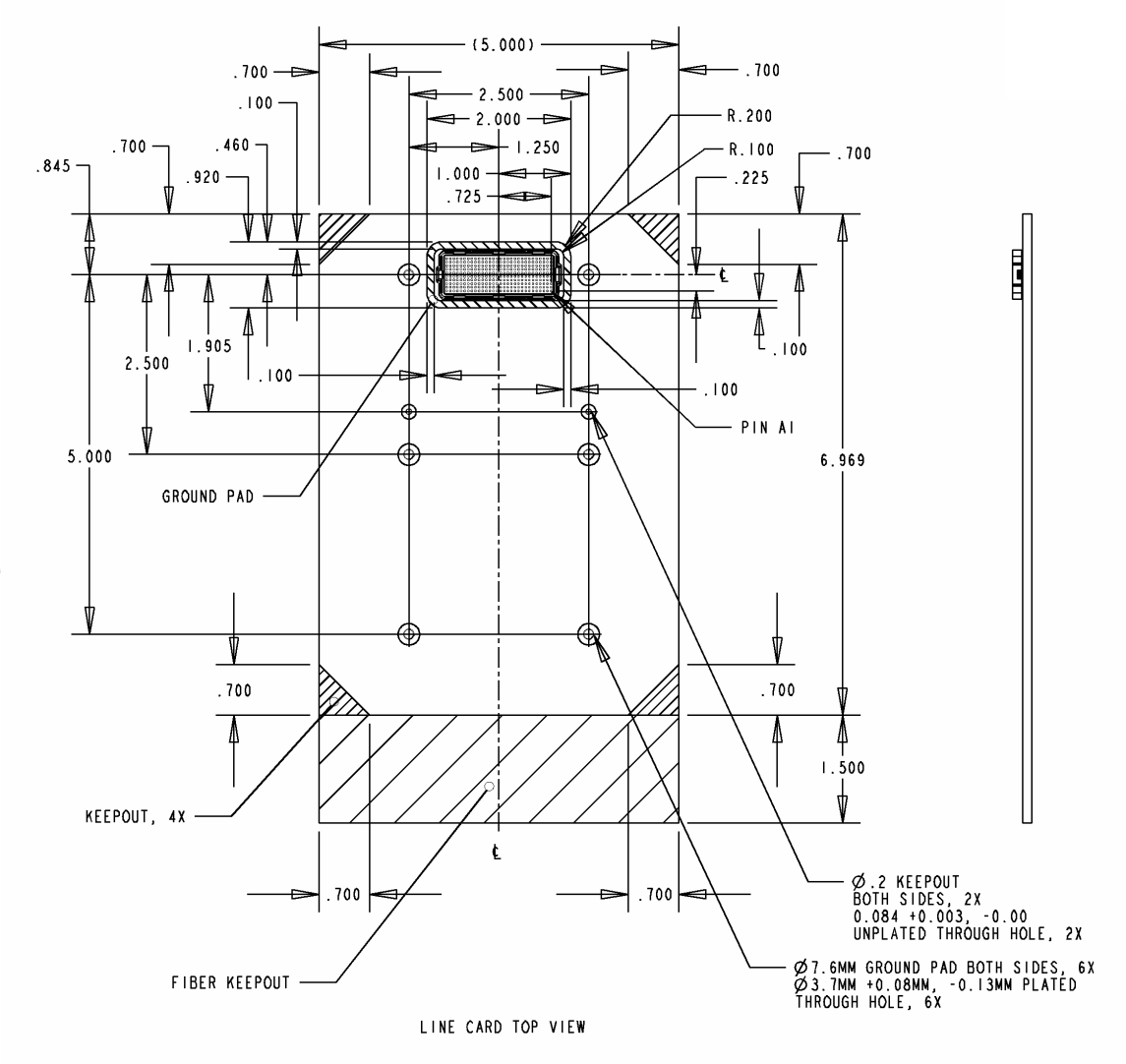


Figure 17 Line Card Keep-Out Areas

Ordering Information

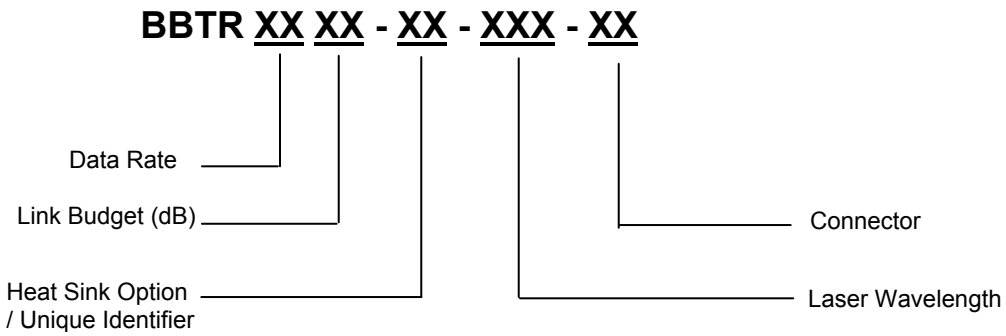


Figure 18 Part Ordering Structure

Table 24 Device Ordering Information*

Parameter	Option Designator	Option	Comment
Data Rate (Gb/s)	40 43	40Gb/s 43Gb/s	The 43G transponder will operate at either 40Gb/s or 43Gb/s - user selectable
Link Budget (dB)	05	5 dB Link (SR1)	
Heat Sink Option / Unique Identifier	N1 L1 H1	No Heat Sink Longitudinal Fins Horizontal Fins	Any customer specific packages will be specified with a unique identifier code in this location
Laser Wavelength (Given as C or L plus absolute frequency in units of 100GHz per ITU Grid)	C00 C01 ….	Currently only C00 is available	Eg 1554.94 nm = 192800 GHz so the wavelength code is C28. C00 means C band but no specific wavelength
Connector	LC SC FC	LC UPC SC UPC FC UPC	Default value is SC

*Other device options may be available. For additional ordering information, please contact a Big Bear Networks account manager at (408) 524-5128 or sales@bigbearnetworks.com.

Optical Safety

This module is a Class 1 laser product with Class 3R laser emissions per standard IEC60825-1:1993 + A1:1997 + A2:2001. The transponder module is affixed with the warning label as shown in Figure 19 below.

Caution - use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

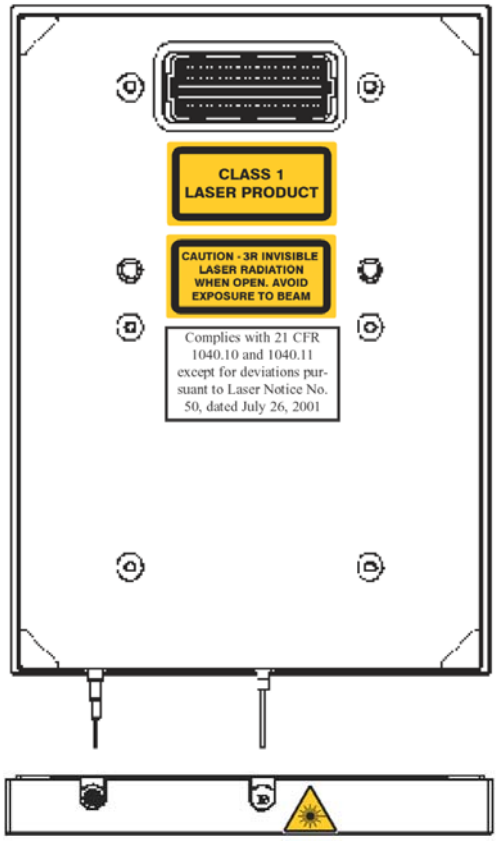


Figure 19: Location of Laser Safety Labels, Certification Label, and Laser Emission Label

Reliability and Qualification

To ensure high product reliability and customer satisfaction, Big Bear Networks has developed a comprehensive Quality and Reliability program. All Transponders are qualified to Big Bear Networks internal standards using MIL-STD-883 test methods and procedures and sampling techniques consistent with Telcordia Technologies requirements. This program characterizes and qualifies components and products starting at the design phase, through the manufacturing process. The qualification test requirements are designed based on the following industry standards:
IC components based on GR-357-CORE
Opto-electronic components based on GR-468-CORE
Transponders subassemblies based on applicable criteria from GR-63-CORE (subsystem) and
GR-468 (opto-electronic devices).

Table 25 Kodiak Reliability and Quality Testing

Parameter	*Standard*
Shock	Tested Per MIL-STD-883 Method 2002, 500 G, 1.0 ms, 5 times/axis (Table 6, GR-468)
Vibration	20G, 20-2,000 Hz, 4min/cy, 4 cy/axis (Table 6, GR-468)
Fire Spread	Meets GR-63-Core sect. 4.2

Contact Big Bear Networks for further detail on our product qualification plans and reliability specifications.

References

The following references are provided for informational purposes only. The parameters and operational behavior outlined in this specification describe the complete functionality of the Kodiak Transponder. Contact Big Bear Networks for any items concerning the operational characteristics of this device.

1. Optical Internetworking Forum, OIF-SxI-5-01.0, “System Interface Level 5 (SxI-5): Common Electrical Characteristics for 2.488 - 3.125Gbps Parallel Interfaces”, October, 2002.
2. Optical Internetworking Forum, OIF-SFI5-01.0, “SerDes Framer Interface Level 5 (SFI-5) - Implementation Agreement for 40Gb/s Interface for Physical Layer Devices”, January 29, 2002.
3. 40Gb/s MSA document “Reference Document for 300 PIN 40Gb Transponder”, Public Document Edition 3, Issued July 19, 2002.
4. ITU-T Recommendation G.693, “Optical interfaces for intra-office systems”, October 2001.
5. Draft ITU-T Recommendation G.8251, “The Control of Jitter and Wander within the Optical Transport Network (OTN)”, Revision 4.0, October, 2001
6. ITU, Recommendation G.707/Y.1322, "Network Node Interface For The Synchronous Digital Hierarchy", April, 2000.
7. ITU, Draft Recommendation G.709 Issue 1.0, “Network Node Interface for the Optical Transport Network (OTN)”, February 2001.
8. ITU, Recommendation G.957 "Optical Interfaces for Equipments and Systems Relating to the Synchronous Digital Hierarchy", June 1999.
9. Philips Semiconductors, "The I^2C-bus Specification", Version 2.1, January 2000.

Appendix A: I²C Interface Protocol

This I²C interface specification for the Kodiak Transponder adheres to the specifications given in the document *"I²C REFERENCE DOCUMENT FOR 300 Pin MSA 10G and 40G TRANSPONDER"*, edition 3, issued July 24, 2002.

A.1 Scope

The protocol is made up of two segments:

1. The 40G MSA Section describing the protocols and commands defined for all the modules compliant with the MSA requirements.
2. The Big Bear Networks vendor Supplier Reserved Commands describing the additional set of commands which have been defined specifically for the Big Bear Networks Kodiak transponder. (see section A.3.2)

Additionally, some of the commands require entering a particular mode, called the *protected mode*, in order to become available for use. This feature is implemented in order to avoid either unsafe access to some commands (those that may alter the module function) or unauthorized access to vendor specific commands.

Note: the 'C' language prefix '0x' is used throughout this document to indicate hexadecimal numbers.

A.2 DATA LINK BASIS

A.2.1 Physical Layer

The data link physical layer complies with the Philips specifications as defined in the *I²C-Bus Specification, Version 2.1, January 2000.*

A.2.1.1 Mechanical Interface

The I²C mechanical interface is five pins within the 300 pin connector. The I²C interface bus on the Kodiak transponder adheres to the MSA document *Reference Document for 300 Pin 40G Transponder*. See Table 5 in the main section of this Kodiak specification document for further description of the bus implementation in the Kodiak transponder.

A.2.1.2 Electrical Interface

A.2.1.2.1 SCL/SDA

The I²C interface on the Kodiak transponder adheres to the *I²C-Bus Specification, Version 2.1, January 2000.* Further detail on the Kodiak I²C electrical interface can be found in the following sections of this specification document:

- *Table 14 I2C Electrical Characteristics (DC)*
- *Table 15 I2C Electrical Characteristics (AC)*

A.2.1.2.2 Address

Address pins are of LVTTL type, positive logic, with a 1K Ohm pull-down resistor internal to the transponder. Unconnected signals will therefore be set to logical '0'. Note that a module's address is sampled once at power-up and any further change is not taken into account until the next power-up.

A.2.1.3 Functional and Procedural Definitions

In order to separate logical messages, special start and stop conditions are created on the I²C bus. The start and stop conditions are as defined in Section 6.2 of the Philips *I²C-Bus Specification.*

A.2.1.4 Bus Mastering

The transponder is connected to the bus as a slave. This means that the host controller is the bus master and:

1. The clock is provided by the host for both transmit and receive frames.
2. Address + r/w byte, as well as start and stop bits are provided by the master.

A.2.1.5 Flow Control

Wait state generation is done in accordance with Section 8.3 in the Philips *I²C-Bus Specification.* Further, the single bit wait state does not exceed 3 consecutive minimum rate bit times. A byte wait state does not exceed the time of 1 minimum rate byte (9 bits including the acknowledge or 100 microseconds with a minimum rate of 90 kHz).

A.2.1.6 Error Handling (Host Timeout)

If the transponder detects a host timeout during a message it resets to being not addressed and begins searching for a START Condition.

A.2.1.7 Response Retention and Retransmission

The last response by the transponder is held in its volatile memory until it receives another command. This allows the host to ask for retransmission of the last response should an error occur. If the transponder is asked for a completely processed response multiple times without intervening commands, the last response is sent again. A *Command Not Executed* response is sent if there have been no previous responses sent since boot-up.

A.2.2 Data Link Layer

For the remainder of the document, transfers from the Host to the transponder Module are noted by: H ->M.
Bytes transferring from the Module to the Host are noted by: M -> H.

A.2.2.1 Message Frame

The messages are binary strings of variable length encapsulated by the I²C hardware link management.
The host <-> device communication is broken down in two successive phases:

1. The host sends a message containing a command with its operands;
2. The device **always**[1] replies to this command when read by the host by sending a message containing a status byte and required data.

It is up the host to check the returned status byte to verify the command completion. The typical host command frame is as follows:

H->M	H->M	H->M	H->M
start	address + *wr* bit	command issued by host	stop

First byte: This is the I²C standard 7 bits slave address for the module plus *wr* bit.
Following bytes: This is the message body, which contains the command and its operands as well as the check byte.

The typical device reply frame is as follows:

H->M	H->M	M->H	H->M
start	address + *rd* bit	data returned by the device	stop

First byte: This is the I²C standard 7 bits slave address for the device plus *rd* bit (generated by the host).
Following bytes: This is the message body, which contains the data returned by the module as well as the check and status bytes (generated by the transponder).

A.2.2.2 ACK/NAK Process

Each transmission has an Acknowledge process at the I²C hardware level. The NAK is provided by the I²C hardware in case of failure.

[1] There are exceptions to this rule listed in the following paragraphs

A.2.3 Data Exchange Basis

The serial link protocol is based on a handshake process, each command issued by the master host being followed by a reply from the addressed module after command execution completion.

This rule accepts some exceptions:
1. A command issued in broadcast mode (only available for *Enhanced Mode*) never leads to a reply from the accessed modules (because they are several);
2. A dynamic address allocation command issued to a new (never allocated) module never leads to a reply from the accessed module (because of resulting address change).

All other commands are based on a command/reply scheme.

A.2.4 Device Addressing

A.2.4.1 Standard Mode

The standard mode is based on the I^2C addressing capability: the transponder only responds to an I^2C message when its own address and the address field of the I^2C frame match. The definition of the address is xxxxyyy. The four most significant bits, xxxx, are 1000 (allocated by Philips). The three least significant bits, yyy, are specific to an individual transponder and constitute the I^2C address offset.

A.2.4.2 Enhanced Mode

The Kodiak transponder does not support enhanced mode at this time.

A.2.4.3 Device Identifier/Module Allocation Process

The module's I^2C address offset is set by the 3 hardware address pins on the 300 pin connector. The device identifier, used in enhanced mode is dynamically allocated using the protocol defined below. A new module (non-allocated) shall never respond to any command. The allocation process is required prior to the activation of the module's I2C bus.

A.2.4.3.1 Standard Mode

1. When the transponder is connected to the existing I^2C bus it first waits for an *Allocate Module* command with no operand (the address shall match the pin-programmed one). This command is expected to be issued by the host in standard mode format.
2. The host verifies the transponder availability using the *Get Module Status* command. Changing the device address is possible by setting the hardware address pins on the 300 pin connector to the expected value and performing a power-down/power-up or module reset sequence.

A.2.5 Data Checking

Additional check processes are provided in order to ensure message consistency and data checking.

The message frame is made of the following parts:

1. A CMD byte (host ➠ module) which contains the code of the command to be executed by the module, or a STS byte (module ➠ host) which contains the status byte of the module, giving information about the last received command completion status;
2. A LGTH byte which contains the length of the command parameters field (may be 0, up to 18);
3. An optional command parameters field, which size and definition depends on the command (each command is associated with a unique size/definition for this field);
4. A CHK byte, which contains the message check byte.

Standard Mode

Command (from host to module, 0 ≤ LGTH ≤18):

Command	*Length*	*Command Parameters Field (0~18 bytes)*				*Check Byte*
CMD	LGTH	DATA1	DATA2	….	DATAn	CHK

Reply (from module to host, 0 ≤ LGTH ≤18), issued either after command completion or error detection:

Command	*Length*	*Reply Parameters Field (0~18 bytes)*				*Check Byte*
STS	LGTH	DATA1	DATA2	….	DATAn	CHK

Both command and reply messages are at least 3 bytes long (Command/status + Length + Check byte).

A.2.5.1 Command Check Byte Calculation

All bytes are XORed in the order transferred then 1 is subtracted, starting from the I^2C 7-bit address + *wr* bit and ending with the last byte prior to the check byte. Should the value of the XOR before the subtraction be 0, the result should be the two's complement of –1 (0xFF). Example:

H→M

ADDR	CMD	LGTH	DATA	DATA	CHK
0x80	Ox44	0x02	0x03	0xFF	0x39

Calculation (in hex): 80 ⊕ 44 ⊕ 02 ⊕ 03 ⊕ FF = 39.

A.2.5.2 Status Check Byte Calculation

When the master performs a read of the slave all of the bytes transferred are subject to the check byte, regardless of direction. The transponder starts it's check byte calculation with the 7-bit read address + *rd* bit it receives. It then proceeds to continue the XOR process across the status, length, and data bytes before transmitting the check byte.

The host knows what transponder address it sent and starts its check byte calculation with the 7-bit read address + *rd* bit it sent out. The host then proceeds to continue the XOR process across the received status, length, and data bytes. It can then compare its result to the received check word.

The check byte is calculated by XORing all bytes in the order transferred, then 1 is subtracted. Should the value of the XOR before the subtraction be 0, the result should be the two's complement of –1 (0xFF). Example (both host and module perform same calculation):

H→M

ADDR
0x81

M→H

STS	LGTH	DATA	DATA	CHK
0x80	0x02	0x03	0xFF	0x39

Calculation (in hex): 81 ⊕ 80 ⊕ 02 ⊕ 03 ⊕ FF = FE.

A.2.6 Status Replying

The transponder module issues a Status Byte (STS) within its reply to a command. The most significant bit of the status byte indicates the Command Processed Number (CPN). The bit alternates between zero and one with each successful message processed by the module. In other words, every time that a status of "OK, Command Executed" is posted to the read buffer, the CPN is toggled. It is not toggled again until another command has been received and successfully executed by the module. Any command received by the module that causes an error status does not toggle the CPN. The CPN is set to zero on module reset and on module allocation. If the host wishes to synchronize with the module, it can issue a "Read Link Status Byte" command. The CPN will be part of the status returned. The host can then set it's tracking of the CPN to the returned value.

The purpose of the CPN is to avoid host confusion on commands dropped because of errors in the address. Example:

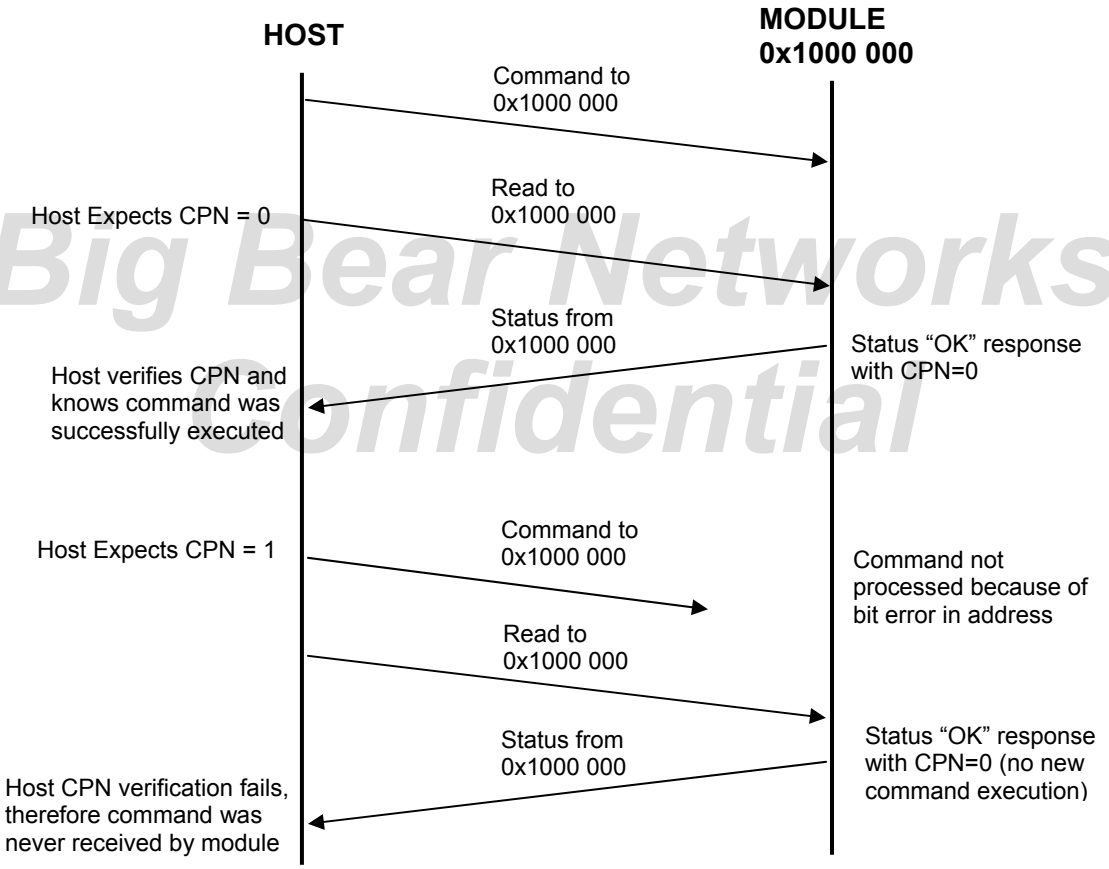


Figure A1: Execution Example of the Command Process Number

The Status Byte can have the following values depending on the module current status:

Status bit 7 (CPN)	Status bits 6-0 (Hex)	Description	Note
0,1	00	OK	Command executed.
0,1	01	Unknown command	The command code is either not supported or is a protected one accessed without having entered the protected mode.
0,1	02	Frame error	The length of the command message (host to module) is not consistent with the value indicated by the Length Byte.
0,1	03	Out of range	At least one parameter of the command is out of range.
0,1	04	Time out	The command timing is out of range.
0,1	05	Check error	The command check byte is not consistent with the value indicated by the Check Byte.
0,1	06	Reserved	Reserved for Future Use
0,1	07	Module busy	The module has started working on the received command (this status only applies for long delay commands, it shall be re-asked later to check the command completion). This reply will only be issued when the module processing the long command is read without an intervening command. Example: Host writes Set Laser ITU Channel command, host reads module, module replies busy.
0,1	08	Still processing	The module is not able to execute the command because the previous one is still in progress. This reply will only be issued following a command write to a module that has yet to complete the previous command. Example: Host writes Set Laser ITU Channel command, host writes Read Laser Bias Current Monitor command, host reads module, module replies still processing (module will continue to reply still processing until the original Set Laser ITU Channel command has either completed successful or failed).
0,1	09	Command not executed	The module is not able to execute the command according to current conditions (for example: a control command is issued while in allocated mode).
0,1	0A-7E	Reserved	Reserved for future use.
0,1	7F	Invalid	Invalid response, 0xFF indistinguishable from no response.

A.2.7 Protection

Some commands are protected against either involuntary or unauthorized access. The protection feature supports two levels of protection:

- The first level, intended for involuntary access to commands that may alter the module's functions, requires one to enter the protected mode but does not require use of a password;
- The second level, intended to protect vendor's specific commands access, requires entering the protected mode with a password.

The protection status is volatile and is always reset to non-protected mode at system power-up.

A.2.8 Module Reset

For all causes of a module reset (power cycle or hardware reset via the MSA connector) the module configuration returns to the last known values of the command registers.

A.3 40G Application Layer

As is required in the base I^2C ICD, the module is exclusively a command/response device. The host always initiates all exchanges. Protected commands that require entering the protected mode prior to being called are indicated by the symbol . The vendor level of protection is marked with the symbol .

Table A.3-1. Module Command List

Command (hex)	Protection	Description
00 to 0F		Reserved for future use
10 to 1F		Reserved for future use
20 to 2F		Reserved for future use
30 to 3F		Reserved for future use
40		Set TX command register
41		Read TX command register
42		Save TX command register
43		Restore TX command register
44		Set RX command register
45		Read RX command register
46		Save RX command register
47		Restore RX command register
48		Reserved for future use
49		*Set Laser ITU Channel (Not Supported)*
4A		*Read Laser ITU Channel (Not Supported)*
4B		*Set Receive Decision Threshold (Not Supported)*
4C		*Read Receive Decision Threshold (Not Supported)*
4D		*Set Demux Phase Offset (Not Supported)*
4E		*Read Demux Phase Offset (Not Supported)*
4F		Set Configurable Alarm
50		Read Configurable Alarm
51 to 5F		Reserved for future use
60		Laser bias current monitor
61		Laser output power monitor
62		Laser temperature monitor
63		*Receiver Signal Monitor AC Optical Power (Not Supported)*
64		Receiver signal monitor average optical power
65		*Laser Wavelength Monitor (Not Supported)*
66		Transponder Temperature Monitor
67		*Photodiode Temperature Monitor (Not Supported)*
68		*Modulator Bias Monitor (Not Supported)*
69		*Read Error Checker Count (Not Supported)*
6A to 6F		*Reserved for future use*

Command (hex)	Protection	Description
70 to 7F		Reserved for future use
80		Read TX alarm status register
81		Read RX alarm status register
82		Read Power Supply Alarm Register
83		Set Rx Interrupt Alarm Mask Register
84		Read Rx Interrupt Alarm Mask Register
85		Set Tx Interrupt Alarm Mask Register
86		Read Tx Interrupt Alarm Mask Register
87 to 8F		Reserved for future use
90 to 9F		Reserved for future use
A0		Read supplier identifier code
A1		Read module type code
A2		Read customer parameter
A3		Write customer parameter
A4 to AF		Reserved for future use
B0 to BF		Reserved for future use
C0		Read Link Status Byte
C1		Enter Non-Allocated Mode
C2		Read maximum I^2C rate
C3		Enter protected mode
C4		Exit protected mode
C5		Allocate Module
C6 to CF		Reserved for future use
D0 to DF		Reserved for future use
E0 to EF		Reserved for future use
F0 to FF		***Supplier reserved codes***
F0		*Supplier reserved codes*
F1		*For Big Bear Internal Use only*
F2		*Big Bear Data Register*
F3		Big Bear Manufacturing Data Register
F4-FF		*For Future Use by Big Bear*

A Note on Register Volatility
The volatility of the registers is indicated in Table A.3-2 below. All non-volatile registers are stored in non-volatile memory which is retained during a power cycle or during the hardware resets 'Module Reset' or 'Register Reset'. Volatile registers will revert to default settings during these same hardware cycles.

The maximum status response time for non-volatile registers is 20msecs. The maximum status response time for volatile registers is 1msec

Table A.3-2 Register Volatility

Register	Type
Tx Command Register	Non-Volatile
Rx Command Register	Non-Volatile
Set Config Alarm Register	Non-Volatile
Customer Parameter Register	Non-Volatile
Manufacturing Data Register	Non-Volatile

Register	Type
Tx Interrupt Alarm Mask Register	Volatile
Rx Interrupt Alarm Mask Register	Volatile

A.3.1 Module Specific Customer Accessible Commands

A.3.1.1 Command Codes

A.3.1.1.1 Set TX Command Register

Sets the module's TX command register. This value is nonvolatile.

H→M					*M→H*	
CMD	LGTH	DATA	DATA	DATA	STS	LGTH
0x40	0x03	Data1	Data2	Data3	STS	0x00

3 Byte operand with MSByte first. DataX options are given in Table A.3.1.1.1-1 below.

Table A.3.1.1.1-1. Tx Command Register Bit Assignments

Data	Bit	Name	Condition	Default
Data1	0	PRBSEN (enables PRBS generator) (NOT SUPPORTED)	0 for PRBS mode 1 for normal operation	1
	1	PRBSPAT0 (selects PRBS pattern length) (NOT SUPPORTED)	Pat1 / Pat0 / Pattern 0 / 0 / 2^7 0 / 1 / 2^{11} 1 / 0 / 2^{23} 1 / 1 / 2^{31}	1
	2	PRBSPAT1 (selects PRBS pattern length) (NOT SUPPORTED)		1
	3	TxDESKEWEN (enables Tx SFI-5 deskew algorithm) (NOT SUPPORTED)	0 for disable 1 for enable	1
	4 ~ 7	FFU		all 1's
Data2	0	TxDCKSEL (selects TxDCK frequency) (NOT SUPPORTED)	0 for TxDCK = $f_{edata}/4$ 1 for TxDCK = f_{edata}	0
	1	TxLINETIMSEL (selects line timing mode)	0 for line (recovered) timing mode 1 for normal (local source) operation	1
	2	TxLLOOPENB (enables line loopback) (NOT SUPPORTED)	0 for enable line loopback 1 for normal operation	1
	3	TxRESET (Mux system reset)	0 for Reset 1 for normal operation (Note 2)	1
	4	TxFIFORES (Mux FIFO reset) (NOT SUPPORTED)	0 for Reset 1 for normal operation	1

	5	AUTOTxFIFORES (Automatic Mux FIFO reset) (NOT SUPPORTED)	0 for auto reset on error 1 for auto reset not enabled	1
	6	SCTxRESET (Self-Clearing Mux System Reset. (NOT SUPPORTED)	0 for Reset 1 for normal operation	1
	7	FFU		1
Data3	0	LsENABLE (laser enabled or disabled)	0 for normal operation 1 for laser disable (Note 3)	0
	1	TxRATESEL0 (rate selection of transmit chain - only 39.8 Gbps rate supported)	Sel1 / Sel0 / Rate (Gbps): 0 / 0 / Invalid 0 / 1 / Invalid 1 / 0 / Invalid 1 / 1 / 39.8(SONET)	1
	2	TxRATESEL1 (rate selection of transmit chain - only 39.8 Gbps rate supported)		1
	3	TxREFSEL (selects TxREFCLK) (NOT SUPPORTED: 622 MHz REQUIRED)	0 for TXREFCLK = $f_{edata}/4$ 1 for TXREFCLK = f_{edata}	1
	4~6	FFU		1
	7	TxMUTEMCLK (mutes the TXMCLK)	0 for TXMCLK mute 1 for normal operation	0

NOTE 1 : f_{edata} is defined to be the single data channel input/output electrical data rate (2.488 Gbps at SONET/SDH)

NOTE 2: The TxRESET 'off' command can be sent immediately after the TxRESET 'on' command. As per the description of MOD_RESET in Table 2 the transponder is fully operational within 500ms of releasing the TxRESET bit.

NOTE 2 : Laser enable is controlled by both a hardwired pin on the Megarray connector and by an I^2C command. The LsEnable hardware pin and LsEnable bit are 'OR'd according to the following truth table:

Table A.3.1.1.1-2. Laser Enable Truth Table

LsEnable bit	LsEnable Pin	Laser output
0	0	0, Enabled
0	1	1, Disabled
1	0	1, Disabled
1	1	1, Disabled

NOTE 3 : Selection of local or recovered timing is controlled by both a hardwired pin on the Megarray connector and by an I^2C command. The TXCKSEL hardware pin and TxLINETIMESEL bit are 'OR'd according to the following truth table:

Table A.3.1.1.1-3. Transmit Timing Truth Table

TxLINETIMESEL bit	TXCKSEL Pin	Transmit (CMU)Timing
0	0	0, Recovered (line) Timing
0	1	1, Local Timing
1	0	1, Local Timing
1	1	1, Local Timing

A.3.1.1.2 Read TX Command Register

H→M		*M→H*				
CMD	LGTH	STS	LGTH	DATA	DATA	DATA
0x41	0x00	STS	0x03	Data1	Data2	Data3

3 Bytes returned with MSByte first.
The DataX description for Read TX Command Register is identical to the *Set TX Command Register* commands in Table A.3.2.1.1-1.

A.3.1.1.3 Save TX Command Register

Saves the current TX command register value in a unique location of the module's nonvolatile memory. The data stored by this command can only be retrieved by the "Restore Tx Command Register" command. Saving the current register values via this command has no effect on values used after the module is reset (per the MSA, the transponder parameters return to last operating state following a reset). The command has no operands.
NOTE: the transponder is limited to less than 10,000 save cycles for the Save TX Command Register.

H→M		*M→H*	
CMD	LGTH	STS	LGTH
0x42	0x00	STS	0x00

A.3.1.1.4 Restore TX Command Register
Restores the TX command register with the value previously stored using the Save TX Command Register command. No operands.

H→M		*M→H*	
CMD	LGTH	STS	LGTH
0x43	0x00	STS	0x00

A.3.1.1.5 Set RX Command Register
This command sets the module's RX command register. This value is nonvolatile. Saving the current register values via this command has no effect on values used after the module is reset.

H→M					*M→H*	
CMD	LGTH	DATA	DATA	DATA	STS	LGTH
0x44	0x03	Data1	Data2	Data2	STS	0x00

3 byte operand with MSByte first.
DataX description for *Rx Command* is given in Table A.3.1.1.5-1 below:

Table A.3.1.1.5-1. Rx Command Register Bit Assignments

Data	Bit	Name	Condition	Default
Data1	0-7	FFU		All 1's
Data2	0	RxMUTE Dout (Mutes the RxDout[0:15]) (NOT SUPPORTED)	0 for mute 1 for normal operation	1
	1	RxDLOOPENB (diagnostic loopback) (NOT SUPPORTED)	0 for line timing mode 1 for normal operation	1
	2	SCRxRESET (Self-Clearing DeMux system reset) (NOT SUPPORTED)	0 for reset 1 for normal operation	1
	3	PRBSEN (enables PRBS checker) (NOT SUPPORTED)	0 for PRBS mode 1 for normal operation	1
	4	PRBSPAT0 (NOT SUPPORTED)	Pat1 / Pat0 / Pattern: 0 / 0 / 2^7 0 / 1 / 2^{15} 1 / 0 / 2^{23} 1 / 1 / 2^{31}	1
	5	PRBSPAT1 (NOT SUPPORTED)		1
	6~7	FFU		All 1's
Data3	0	RxRATESEL0 (rate selection of receive chain - only 39.8 Gbps rate supported)	Sel1 / Sel0 / Rate (Gbps): 0 / 0 / Invalid 0 / 1 / Invalid 1 / 0 / Invalid 1 / 1 / 39.8(SONET)	1
	1	RxRATESEL1 (rate selection of receive chain- only 39.8 Gbps rate supported)		1
	2	RxREFSEL (selects RxREFCLK frequency) (NOT SUPPORTED: 622 MHz REQUIRED)	0 for RxREFCLK = $f_{edata}/4$ 1 for RxREFCLK = f_{edata} NOTE 1	1
	3	RxLCKREF (Locks RxDCK to RxREFCLK)	0 locks RXDCK to RXREFCLK 1 for normal operation	1
	4	RxMCLKSEL (selects RxMCLK frequency) (RxMCKL is NOT SUPPORTED)	0 for RxMCLK = $f_{edata}/4$ 1 for RxMCLK = f_{edata}	1
	5	RxRESET (DeMux system reset)	0 for Reset 1 for normal operation (Notes 2 & 3)	1
	6	RxMUTERxDCK (mutes the RxPOCLK) (NOT SUPPORTED)	0 for RxDCK mute 1 for normal operation	1
	7	RxMUTEMCLK (mutes the RxMCLK) (RxMCKL is NOT SUPPORTED)	0 for RXMCLK mute 1 for normal operation	1

NOTE 1: f_{edata} is defined to be the single data channel input/output electrical data rate (2.488 Gbps at SONET/SDH)

NOTE 2: RxRESET holds in reset until commanded to release the reset condition

NOTE 2: The RxRESET 'off' command can be sent immediately after the RxRESET 'on' command. The transponder is fully operational within 10ms of releasing the RxRESET bit.

A.3.1.1.6 Read RX Command Register

H→M

CMD	LGTH
0x45	0x00

M→H

STS	LGTH	DATA	DATA	DATA
STS	0x03	Data1	Data2	Data3

3 Bytes Returned, MSByte first

The DataX description for the Read RX command is identical to the *Set RX Command Register* command as shown in Table A.3.1.1.5-1.

A.3.1.1.7 Save RX Command Register

Saves the current RX command register value in a unique location of the module's nonvolatile memory. The data stored by this command can only be retrieved by the "Restore Rx Command Register" command. Saving the current register values via this command has no effect on values used after the module is reset (per the MSA, the transponder parameters return to last operating state following a reset). The command has no operands.
NOTE: the transponder is limited to less than 10,000 save cycles for the Save RX Command Register.

H→M		*M→H*	
CMD	LGTH	STS	LGTH
0x46	0x00	STS	0x00

A.3.1.1.8 Restore RX Command Register

Restores the RX command register with the value previously stored using the Save RX Command Register command.
No operands.

H→M		*M→H*	
CMD	LGTH	STS	LGTH
0x47	0x00	STS	0x00

A.3.1.1.9 Set Laser ITU Channel
Not Supported

A.3.1.1.10 Read Laser ITU Channel
Not Supported

A.3.1.1.11 Set Receive Decision Threshold
Not Supported

A.3.1.1.12 Read Receive Decision Threshold
Not Supported

A.3.1.1.13 Set Demux Phase Offset
Not Supported

A.3.1.1.14 Read Demux Phase Offset
Not Supported

A.3.1.1.15 Set Configurable Alarm

H→M			*M→H*	
CMD	LGTH	DATA	STS	LGTH
0x4F	0x01	Data1	STS	0x00

1 Byte Operand

Table A.3.1.1.15-1. Mapping to CFG_ALM

Data	Value	Alarm Name
Data1	0	Rx POWALM (Loss of average optical power)
	1	RxLOCKERR (Loss of RxPLL lock indicator)
	2	RXS (SFI-5 DEMUX Status)
	3	LsBIASALM (Laser bias current alarm)
	4	LsTEMPALM (Laser temperature alarm)
	5	TxLOCKERR (Loss of TxPLL lock alarm)
	6	TxFIFO ERR (Mux FIFO error indicator) (NOT SUPPORTED)
	7	TXOOA (SFI-5 Deskew Alarm)
	8	PRBSERRDET (an error was detected by the PRBS error checker) (NOT SUPPORTED)
	9	PRBSCntHalfFull (PRBS error counter register is half full) (NOT SUPPORTED)
	10	EOL (end of life) (NOT SUPPORTED)
	11	PSUMMARY (power supply fault)
	12-239	FFU
	240-255	Vendor Specific

NOTE: The state of the configurable alarm is non-volatile and will be restored to its previous state on power cycle.
NOTE: The initial default state for Data1 is 0, i.e. default is RXPOWALM.

A.3.1.1.16 Read Configurable Alarm

This command reads the present assignment of the configurable alarm pin.

H→M		*M→H*		
CMD	LGTH	STS	LGTH	DATA
0x50	0x00	STS	0x01	Data1

1 Bytes Returned: The Data1 value is defined in Table A.3.1.1.15-1.

A.3.1.2 Measurement Codes

The module operation can be monitored using the commands shown in the following table. Details of the command and response are given in sections 3.1.2.1 through 3.2.2.4

Command	Measurement	Units
LsBIASMON	Returns laser bias current	μA
LsPOWMON	Returns laser optical power	μW
LsTEMPMON	Returns laser temperature	m°C
RxSIGMON	Returns AC (modulated) optical signal power (NOT SUPPORTED)	
RxPOWMON	Returns the average received optical power	μW
	Laser Wavelength Returns offset from the exact ITU wavelength (NOT SUPPORTED)	
	Transponder Temperature Monitor Returns ambient temperature inside module	m°C
	Photodiode Temperature Monitor (NOT SUPPORTED)	m°C
	Modulator Bias Monitor (NOT SUPPORTED)	scaled to 16 bits
	Read Error Checker Error Count (NOT SUPPORTED)	errors

A.3.1.2.1 Laser Bias Current Monitor

Returns the laser bias current, LsBIASMON.

H→M		*M→H*				
CMD	LGTH	STS	LGTH	DATA	DATA	DATA
0x60	0x00	STS	0x03	Data1	Data2	Data3

The 3 bytes returned are as follows:

- Data1, Data 2, Data3, MSB first;
- Data Unit: μA;
- Data format: 24 bits two's complement;

A.3.1.2.2 Laser Output Power Monitor

Returns the laser output optical power LsPOWMON.

H→M		*M→H*				
CMD	LGTH	STS	LGTH	DATA	DATA	DATA
0x61	0x00	STS	0x03	Data1	Data2	Data3

The 3 bytes returned are as follows:

- Data1, Data2, Data3, MSB first;
- Data Unit: μW;
- Data format: 24 bits two's complement;

A.3.1.2.3 Laser Temperature Monitor
Returns the laser temperature, LsTEMPMON.

H→M		*M→H*				
CMD	LGTH	STS	LGTH	DATA	DATA	DATA
0x62	0x00	STS	0x03	Data1	Data2	Data3

The 3 bytes returned are as follows:
- Data1, Data2, Data3, MSB first;
- Data Unit: degrees m°C;
- Data format: 24 bits two's complement.

A.3.1.2.4 Receiver Signal Monitor AC Optical Power
Not Supported.

A.3.1.2.5 Receiver Signal Monitor DC Power
Returns the average received optical power, RxPOWMON.

H→M		*M→H*				
CMD	LGTH	STS	LGTH	DATA	DATA	DATA
0x64	0x00	STS	0x03	Data1	Data2	Data3

The 3 bytes returned are as follows:
- Data1, Data2, Data3, MSB first;
- Data Unit: µW;
- Data format: 24 bits two's complement.

NOTE: The value returned by the RxPOWMON command is specified to be valid in the range of -8dBm to +3dBm, with an accuracy (including measurement uncertainty) of ± 0.7dB.

A.3.1.2.6 Laser Wavelength Monitor
Not Supported

A.3.1.2.7 Transponder Temperature Monitor
Returns the ambient circuit card temperature within the module.

H→M		*M→H*				
CMD	LGTH	STS	LGTH	DATA	DATA	DATA
0x66	0x00	STS	0x03	Data1	Data2	Data3

The 3 bytes returned are as follows:
- Data1, Data2, Data3, MSByte first;
- Data Unit: m°C;
- Data format: 24 bits two's complement.

A.3.1.2.8 Photodiode Temperature Monitor
Not Supported

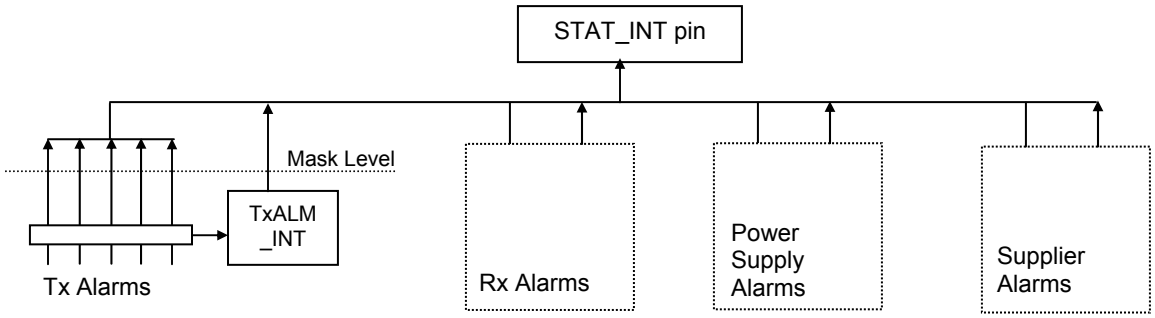
A.3.1.2.9 Modulator Bias Monitor
Not Supported

A.3.1.2.10 Read Error Checker Error Count
Not Supported

A.3.1.3 Alarm Codes

The module alarm status can be monitored using the following commands:

The hierarchy of ALM_INT states flowing to the STAT_INT pin on the 300 pin connector is shown below. The structure shown for Tx Alarms is also used for Rx Alarms, Power Supply Alarms, and Supplier Alarms.



A.3.1.3.1 Read TX Alarm Status Register

H→M		*M→H*				
CMD	LGTH	STS	LGTH	DATA	DATA	DATA
0x80	0x00	STS	0x03	Data1	Data2	Data3

The 3 bytes returned are as shown in Table 3.1.3.1-1 below

Table 3.1.3.1-1. Tx Alarm Status Register Bit Assignment

Data	Bit	Name	Condition
Data1	0~7	FFU	0xFF
Data2	0	EOLALM (Laser End of Life Alarm) (NOT SUPPORTED)	1
	1	ModTEMPALM (Modulator Temperature Alarm)	0 for alarm active, 1 for normal operation Triggers if measured modulator temperature is outside ± 2C of the temperature set point of 25°C. If measured modulator temperature reaches 35°C the modulator is shut down. When the modulator temperature returns to within ± 2C of the set point the modulator will turn on again.
	2	TxOOA (SFI-5 Deskew Alarm)	0 for alarm active, 1 for normal operation The TxOOA alarm is triggered when three consecutive frames contain errors.
	3	TxLOFALM (Loss of Frame Alarm) (NOT SUPPORTED)	1
	4	TxDWCERR (Latching SFI-5 Deskew Channel error, cleared on read) (NOT SUPPORTED)	1
	5-7	FFU	All bits 1

Data3	0	TxALM INT (Tx Summary Alarm) *Triggered if any Tx alarm is active*	0 for alarm active, 1 for normal operation
	1	LsBIASALM (Laser bias current alarm)	0 for alarm active, 1 for normal operation Triggers if measured current is outside ± 5% of laser bias set point. If measured current reaches 20% over the set point the laser is shut down. A transponder reset (MOD_RESET) is required to recover from this laser shut down state.
	2	LsTEMPALM (Laser temperature alarm)	0 for alarm active, 1 for normal operation Triggers if measured laser temperature is outside ± 2C of the laser temperature set point of 25°C. If measured laser temperature reaches 35°C the laser is shut down. When the laser temperature returns to within ± 2C of the set point the laser will turn on again.
	3	TxLOCKERR (Loss of TxPLL lock indicator)	0 for alarm active, 1 for normal operation When the TxLOCKERR alarm is triggered it causes an automatic TxRESET.
	4	TxFIFO ERR (Mux FIFO error indicator) (NOT SUPPORTED)	0 for alarm active, 1 for normal operation
	5	LsPOWALM (Laser power alarm)	0 for alarm active, 1 for normal operation The LsPOWALM is triggered when the laser power is measured to be below 50% of its initial set point.
	6	ModBIASALM (Modulator Bias Alarm) (NOT SUPPORTED)	0 for alarm active, 1 for normal operation
	7	LATCHEDTxFIFOERR (Historical Mux FIFO error indicator) (NOT SUPPORTED)	0 for alarm since last read, 1 for no alarm since last read or if not implemented (TxRESET, manual TxFIFORESET, or a read of this register resets bit to 1)

NOTE: All the Tx alarms in the table above are all non-latching unless identified otherwise.

A.3.1.3.2 Read RX Alarm Status Register

H→M		*M→H*			
CMD	LGTH	STS	LGTH	DATA	DATA
0x81	0x00	STS	0x02	Data1	Data2

The 2 bytes returned are as shown below in Table A.3.1.3.2-1.

Table A.3.1.3.2-1. Rx Alarm Register Bit Assignment

Data	Bit	Name	Condition
Data1	0~7	FFU	0xFF
Data2	0	RxALM INT (Rx Summary Alarm, with exception to PRBSERRDET) *Triggered if any RX alarm is active except for PRBSERRDET*	0 for alarm active, 1 for normal operation
	1	RxPOWALM (Loss of average optical power alarm)	0 for alarm active, 1 for normal operation RxPOWALM is triggered when the average optical input power is below -10dBm. The alarm operates with 1dB of hysteresis.
	2	RxSIGALM (Loss of AC optical power alarm) (NOT SUPPORTED)	1
	3	RxLOCKERR (Loss of RxPLL Lock) *In the Kodiak Transponder this alarm is the same as RXS, i.e. is enabled when the clock is no longer locked to the incoming data stream.*	0 for alarm active, 1 for normal operation
	4	RXS (SFI-5 DEMUX status) *In the Kodiak Transponder this alarm is enabled when the clock is no longer locked to the incoming data stream.*	0 for alarm active, 1 for normal operation
	5	PRBSERRDET (NOT SUPPORTED)	
	6~7	FFU	111

NOTE: All the Rx alarms in the table above are all non-latching unless identified otherwise.

A.3.1.3.3 Read Power Supply Alarm Status Register

H→M		*M→H*		
CMD	LGTH	STS	LGTH	DATA
0x82	0x00	STS	0x01	Data1

Data1 description is given below in Table A.3.1.3.3-1.

Table A.3.1.3.3-1. Read Power Supply Status Register Bit Assignments

Data	Bit	Name	Condition
Data1	0	PSUMMARY (logical "OR" of bits 1 through 6)	0 for alarm active, 1 for normal operation *When PSUMMARY is active it causes the hardware interrupt STAT_INT to be active.*
	1	P5VANALOG (+5V analog) (NOT SUPPORTED)	0 for alarm active, 1 for normal operation (Note 2)
	2	N5V2ANALOG (-5.2V analog)	0 for alarm active, 1 for normal operation (Note 2)
	3	P3P3VANALOG (+3.3V analog)	0 for alarm active, 1 for normal operation (Note 2)
	4	P3P3VDIGITAL (+3.3V digital)	0 for alarm active, 1 for normal operation (Note 2)
	5	LVDIGITAL (low voltage digital)	0 for alarm active, 1 for normal operation (Note 2)
	6	N5P2VDIGITAL (-5.2V digital)	0 for alarm active, 1 for normal operation (Note 2)
	7	FFU	1

Note 1: All bits shall be non-latching unless specifically identified as latching.
Note 2: All power supply alarms are triggered at ± 7% of the nominal value.

A.3.1.3.4 Set Rx Interrupt Alarm Mask Register

This command inhibits the commanded alarms from contributing to the STAT_INT pin output.

H→M				*M→H*	
CMD	LGTH	DATA	DATA	STS	LGTH
0x83	0x02	Data1	Data2	STS	0x00

DataX description is given in below in Table A.3.1.3.4-1.

Table 3.1.3.4-1. Rx Interrupt Alarm Mask Register Bit Assignment

Data	Bit	Name	Condition
Data1	0~7	FFU	0xFF
Data2	0	RxALM INT (Rx Summary Alarm, with exception to PRBSERRDET)	0 for alarm active, 1 to disable interrupt
	1	RxPOWALM (Loss DC power alarm)	0 for alarm active, 1 to disable interrupt
	2	RxSIGALM (Loss of AC optical power alarm)(NOT SUPPORTED)	1
	3	RxLOCKERR	0 for alarm active, 1 to disable interrupt
	4	RXS	0 for alarm active, 1 to disable interrupt
	5	PRBSERRDET(NOT SUPPORTED)	1
	6~7	FFU	All bits 1

Note that the default state for the alarm mask is '1' (alarm disabled) unless stated otherwise.

A.3.1.3.5 Read Rx Interrupt Alarm Mask Register

The message frame is as follows:

H→M		*M→H*			
CMD	LGTH	STS	LGTH	DATA	DATA
0x84	0x00	STS	0x02	Data1	Data2

DataX description for the Read Rx Interrupt Mask is the same as given in Table 3.1.3.4-1.

A.3.1.3.6 Set Tx Interrupt Alarm Mask Register

This command inhibits the commanded alarms from contributing to the STAT_INT pin output.

H→M					*M→H*	
CMD	LGTH	DATA	DATA	DATA	STS	LGTH
0x85	0x03	Data1	Data2	Data2	STS	0x00

DataX description is given below in Table A.3.2.3.6-1.

Table A.3.1.3.6-1. Tx Interrupt Alarm Mask Register Bit Assignment

Data	Bit	Name	Condition
Data1	0~7	FFU	0xFF
Data2	0	EOLALM (Laser End of Life Alarm) (NOT SUPPORTED)	0 for alarm active, 1 to disable interrupt
	1	ModTEMPALM (Modulator Temperature Alarm)	0 for alarm active, 1 to disable interrupt
	2	TxOOA (SFI-5 Deskew Alarm)	0 for alarm active, 1 to disable interrupt
	3	TxLOFALM (Loss of Frame Alarm) (NOT SUPPORTED)	0 for alarm active, 1 to disable interrupt
	4	TxDWCERR (Latching SFI-5 Deskew Channel error, cleared on read) (NOT SUPPORTED)	0 for alarm active, 1 to disable interrupt
	5-7	FFU	All bits 1
Data2	0	TxALM INT (Tx Summary Alarm)	0 for alarm active, 1 to disable interrupt
	1	LsBIASALM (Laser bias current alarm)	0 for alarm active, 1 to disable interrupt
	2	LsTEMPALM (Laser temperature alarm)	0 for alarm active, 1 to disable interrupt
	3	TxLOCKERR (Loss of TxPLL lock indicator)	0 for alarm active, 1 to disable interrupt
	4	TxFIFO ERR (Mux FIFO error indicator) (NOT SUPPORTED)	0 for alarm active, 1 to disable interrupt
	5	LsPOWALM (Laser power alarm)	0 for alarm active, 1 to disable interrupt
	6	ModBIASALM (Modulator Bias Alarm) (NOT SUPPORTED)	0 for alarm active, 1 to disable interrupt
	7	LATCHEDTxFIFOERR (Historical Mux FIFO error indicator) (NOT SUPPORTED)	0 for alarm active, 1 to disable interrupt

Note that the default state for the alarm mask is '1' (alarm disabled) unless stated otherwise.

A.3.1.3.5 Read Tx Interrupt Alarm Mask Register

H→M		*M→H*				
CMD	LGTH	STS	LGTH	DATA	DATA	DATA
0x86	0x00	STS	0x03	Data1	Data2	Data3

DataX description are the same as given in Table A.3.1.3.6-1.

A.3.1.3.6 Power Supply Interrupt Alarm Mask Register

Though not provided in the MSA, the Kodiak Transponder also has the ability to mask the power supply alarms. This mask is given in the Supplier Reserved Section of the I^2C commands in section 3.2.

A.3.1.4 Identifier Codes

Module identifying information can be read using the following commands:

A.3.1.4.1 Read Supplier Identifier Code

Returns the supplier number.

H→M		*M→H*		
CMD	LGTH	STS	LGTH	DATA
0xA0	0x00	STS	0x01	IC

This will return the Big Bear Networks supplier code of 0x30.

A.3.1.4.2 Read Module Type Code

Returns the module type.

H→M		*M→H*		
CMD	LGTH	STS	LGTH	DATA
0xA1	0x00	STS	0x01	TC

1 byte returned:

- TC (Type Code) is defined as follows:
  - 0x00 for undefined type
  - 0x01 VSR2000-2R1 2km
  - 0x02 VSR2000-3R1 2km
  - 0x03 VSR2000-3R2 2km
  - 0x04 VSR2000-3R3 2km
  - 0x05 VSR2000-3R5 2km
  - 0x06 VSR2000-2L2 2km
  - 0x07 VSR2000-2L3 2km
  - 0x08 VSR 2000-2L5 2km
  - 0x09 VSR2000-3M1 2km
  - 0x0A VSR2000-3M2 2km
  - 0x0B VSR2000-3M3 2km
  - 0x0C VSR2000-3M5 2km
  - 0x0D VSR2000-3H2 2km
  - 0x0E VSR2000-3H3 2km
  - 0x0F VSR2000-3H5 2km
  - 0x10 to 0xFF Reserved for Future Use

For the Kodiak transponder this command will return the code 0x03.

A.3.1.4.3 Read Customer Parameter

This command returns 1 to 16 bytes stored in the 64 bytes customer dedicated area of the module's nonvolatile memory.

H→M				*M→H*				
CMD	LGTH	LGTH	LGTH	STS	LGTH	DATA	....	DATA
0xA2	0x02	ADD	N	STS	N	Data0	....	DataN

2 bytes operand:

- ADD (memory ADDress, range is 0x00 to 0x3F)
- N [number of contiguous bytes to return (0x01 to 0x10, inclusive)]

N bytes returned:

- Data (stored data)

Usage: ADD+ N-1 ≤ 0x3F for the command to be valid.

A.3.1.4.5 Write Customer Parameter

This command shall store 1 to 16 bytes in the 64 bytes customer dedicated area of the module's nonvolatile memory.
NOTE: the transponder is limited to less than 10,000 writes to the Customer Parameter section.

The message frame shall be as follows:

H→M						*M→H*	
CMD	LGTH	DATA	DATA	....	DATA	STS	LGTH
0xA3	0xN+1	ADD	Data1	....	DataN	STS	0x00

N+1 bytes operand:

- ADD (memory ADDress, range is 0x00 to 0x3F)
- Data1:N (Data to store, 0x01<N≤0x10)

Usage: All bytes in a write must reside in the same 16 byte page where a page begins with binary address xx0000 and ends with xx1111.

A.3.1.5 Configuration Codes

The module configuration can be set and monitored using the following commands:

A.3.1.5.1 Read Module Status

This command is provided as a neutral command which purpose is only to return the module status.

The message frame is as follows:

H→M		*M→H*			
CMD	LGTH	STS	LGTH	DATA	DATA
0xC0	0x00	STS	0x01	0xC0	Data1

2 bytes returned:

- Fixed value 0xC0 (echo of command number);
- Data1:
  - Standard addressing mode: Module 7-bit address, left justified with bit 0 cleared to zero (binary 1000yyy0);
  - Enhanced addressing mode: TBD.

The returned data is provided to verify the STS is in response to the Module Status Command, not a prior command. This extra data will allow the host to synchronize the Command Processed Number (CPN) with the module.

A.3.1.5.2 Enter Non-Allocated Mode

This command allows the module to switch to the non-allocated state. There are no operands.

H→M

CMD	LGTH
0xC1	0x00

A.3.1.5.3 Read Maximum I^2C rate

H→M

CMD	LGTH
0xC2	0x00

M→H

STS	LGTH	DATA
STS	0x01	Data1

1 Byte returned

- MBR (Maximum Baud Rate)
  - 0x01: 100kbps
  - 0x04: 400kbps

A.3.1.5.4 Enter Protected Mode

This command allows the module to exit the protected mode. The protected mode is automatically disabled after a protocol processor reset. This command is available either to enter the protected mode (without password) or to enter the Vendor Protected Mode (with password).

To enter Protected Mode the message frame is:

H→M

CMD	LGTH
0xC3	0x00

M→H

STS	LGTH
STS	0x00

To enter the Vendor Protected Mode the message frame is:

H→M

CMD	LGTH	DATA		DATA
0xC3	0x08	K1	....	K8

M→H

STS	LGTH
STS	0x00

Where the 8 byte operand is:

- K1...K8 (eight characters key, vendor defined)

A.3.1.5.5 Exit Protected Mode

This command allows the module to exit the protected mode, thus disabling the protected functions.

H→M

CMD	LGTH
0xC4	0x00

M→H

STS	LGTH
STS	0x00

A.3.2.5.6 Allocate Module

This command allows the module to be activated. At present only 'standard mode' is supported. This command is issued before using the I^2C bus (all other commands) because it activates the data link.

Note: This command is not protected while the module is not allocated.

Standard Mode

The message frame is as follows (no operands):

H→M

CMD	LGTH
0xC5	0x00

Following this command, the module's address is as follows: the Philips allocated address format is 1000YYY and YYY is the value of the 3 address pins on the 300 pin connector, sampled during reset.

A.3.2 Supplier Reserved Commands

The following commands are supplier reserved codes and are specific to the Kodiak Transponder. Most of these commands are protected user codes and protected mode must be entered prior to the command in order to execute ( ), many are also password protected ( )

A.3.2.1Module Manufacturing Data

The public manufacturing data is available through the OxF3 command.

The 'read' command structure is:

H→M

CMD	LGTH	DATA	DATA
0xF3	0x02	0x00	Register

M→H

STS	LGTH	DATA	DATA	……	DATA
STS	0xN	Data1	Data2	……	DataN

The returned data format is a string of bytes with the number of bytes dependent on the specific register.

Register	Returned Data Format
0x00	Vendor Part Number (First Half) String of sixteen ASCII bytes padded on the right with spaces (20h).
0x01	Vendor Part Number (Second Half) String of sixteen ASCII bytes padded on the right with spaces (20h).
0x02	Vendor Revision Number String of four ASCII bytes padded on the right with spaces (20h). A value of all ASCII zeros in the 4-byte field indicates that the vendor revision is unspecified. Note that this revision number changes when any of the following change: Printed Circuit Board Demountable Components on PCB (CMU etc) Programmable Logic Device Mechanical
0x03	Vendor Firmware Revision String of four ASCII bytes padded on the right with spaces (20h). A value of all ASCII zeros in the 4-byte field indicates that the firmware revision number is unspecified
0x04	Vendor Serial Number String of sixteen ASCII bytes padded on the right with spaces (20h). A value of all ASCII zeros in the 16-byte field indicates that the serial number is unspecified.
0x05	Vendor Date Code (Date of Manufacture) String of ten ASCII bytes with the format of XXXXYYZZBB XXXX = year YY = month ZZ = day BB = vendor specific lot code (may be blank)

A.3.2.2 Reading and Writing to Vendor Data Register

The vendor data register allows the user to read and reset several parameters in the Big Bear Networks Kodiak transponder which are not available in the standard MSA section. This register currently operates in protected mode, but without requiring a password.

The 'read' command structure is:

H→M

CMD	LGTH	DATA	DATA
0xF2	0x02	Data1	Data2

M→H

STS	LGTH	DATA	DATA
STS	0x02	Data3	Data4

The command field is defined as:

- Data1, Data2, MSB first.

The returned data format is as follows:

- Data3, Data4, MSB first.

Several of the vendor data registers can be written to using the following command:

H→M

CMD	LGTH	DATA	DATA	DATA	DATA
0xF2	0x04	Data1	Data2	Data3	Data4

M→H

STS	LGTH	DATA	DATA
STS	0x02	Data3	Data4

The command field is defined as:

- Data1,Data2, MSB first = register number
- Data3,Data4, MSB first = value to write

NOTE that the Module returns the values Data3 and Data4 that were actually written to the location.

The returned data parameters are listed below in Table A.3.2.2-1

Table A.3.2.2-1

Register	Data Parameter	Read / Write
0x0000	This register should always be set to '0'. The default value is '0'	Read / Write
0x0001	Set / Read Power Supply Alarm Mask (All are 0 for alarm active, 1 to disable interrupt) Bit 0: PSUMMARY (logical "AND" of bits 1 through 6) Bit 1: P5VANALOG (+5V analog) (NOT USED) Bit 2: N5V2ANALOG (-5.2V analog) Bit 3: P3P3VANALOG (+3.3V analog) Bit 4: P3P3VDIGITAL (+3.3V digital) Bit 5: LVDIGITAL (low voltage digital) Bit 6: N5P2VDIGITAL (-5.2V digital) The default setting is '1', i.e. the alarms are disabled. Bits 7-15 are currently set to '1'	Read / Write
0x0002	Miscellaneous Alarm Status (All bits are '0' for alarm active, and '1' for normal operation) Bit 0: Supplier Alarm Summary Bit 1: Transponder Temperature Alarm Triggers if measured Transponder Internal Ambient temperature reaches 75°C. Bits 2-15 are currently set to '1'	Read Only
0x0003	Alarm Mask (All are '0' for alarm active, and '1' to disable interrupt. Default is '1') Bit 0: Enable Supplier Alarm Summary Bit 1: Enable Transponder Temperature Alarm Bits 2-15 are currently set to '1'	Read / Write

0x0004	Limiting amp threshold control, with range of ± 60mV Data format is mV in S11.4 format. NOTE: when not using the factory default value it is necessary for this command to be sent every time the Tx or Rx registers are written. Otherwise the threshold control will be reset to the factory default.	Read & Write
0x0005 - 0xFFFF	For future use	

END OF I^2C SECTION

Revision History

Revision	Date	Description
0.1	1/1/01	▪ Initial Draft of 40G Transponder
0.1-0.9	1/10/01 to 10/8/01	▪ Incorporated results from several OIF forums over the several months on SFI-5 electrical and de-skew, as well as initial 300 pin connector pin-out ▪ Modified SR optical specifications to align with ITU G.vsr draft.
0.91-0.94	11/13/01 to 3/18/02	▪ Incorporated latest ITU (SR1 & SR2) and OIF (SFI-5 and SxI-5) specification updates and clarified G.693 Jitter requirements ▪ Revised 300pin connector pin out to reflect latest customer requirements ▪ Added RXREFCK as a mandatory reference signal for the Transponder and added the optional monitor clocks (TXMONCK and RXXMONCK) ▪ Revised I^2C to MSA agreement with additional BBN commands ▪ Updated SFI-5 Eye Mask and Jitter Specifications to the OIF2001.149.10 of January 23, 2002
0.95 - 0.97	3/28/02 - 9/20/02	▪ Updated pin specs and I2C to conform with 40G MSA documents in April , May and July, and updated references to OIF-SXI5-01.0 (OCT 2002) issued June 5, 2002. ▪ Increased specification of nominal mechanical height to 0.65" without heatsink and 0.98"with heatsink. ▪ Increased Max Steady State current for 3.3V Analog to 2500 mA from 2000 mA ▪ Added in TXMONCK and updated electrical interface and jitter tolerance on TXREFCK and RXREFCK, TXCSC and RXDSC
0.98	10/9/02	▪ Published 40/43G specification document.
0.98a	10/14/02	▪ Remove SR2
0.98b	11/4/02	▪ Added detail about LOS and RXS behavior ▪ Clarified TXCKSRC DC coupled characteristics (match SxI5) ▪ removed PRBSERRDET from config alarm (i.e. not supported) ▪ changed the 3.3V supply maximum value to 3.6V from 4.0V ▪ changed the 1.8V supply maximum value to 2.0V from 2.4 ▪ slight modification of figure 1 to re-label microprocessor and photo-receiver blocks ▪ Updated references to OIF to now reference the implemented SFI-5 and SxI-5 ▪ Updated new address and phone
0.98c	11/8/02	▪ Put in operating case temperature limit of 0 to 65C. ▪ Minor tidy up changes.
0.98d	11/12/02	▪ Updated Line card drawing ▪ Increased TXREFCK and RXREFCK tolerance to 30ppm ▪ Added a table of alarm response times ▪ Added spec for power supply ripple of 1% (1Hz to 20MHz)
0.99	1/9/03	• Updated the I2C address and drawing and added latency comments • Changed maximum power consumption to 32W from 30W • Changed alarm mask default to be that all alarms are masked at default. • Added notes to the config alarm that the settings are non-volatile and default state is zero (i.e. RxPOWALM) • Added in identifier code of 0x30, and module type code of 0x03 • Changed the figure showing the STAT_INT alarm flow - now TxALM_INT etc are not blocking the flow of the alarms to STAT_INT.

		• Changed the modulator and laser temperature alarms to indicate that they will both turn on again once they are within 2C of their set points. • Typical current on 5V analog line reduced to zero (not used). I2C alarm for this changed to 'not supported' • Added Figure showing temperature measurement location • Added TXDCK, TXDSC, RXDCK, RXDSC to the electrical signal table.
0.99a	3/4/2003	• Added hardware-reset minimum hold times of 100ms • Increased REFCLK input range to 400mv – 1800mV p-p differential per 40G MSA • Added Note in section A.3.1 on volatility of registers under resets and power cycle • Added TXMUTEMCLK command to the TX Command Register (Data3, bit 7), and removed this from 0x0000 register of command 0xF2.
0.99c	4/15/2003	• Skipped rev b • Added further clarification on timing response to several of the pin controls and I2C reset commands • Increased the maximum 3.3V analog current to 2700mA • Changed RXPOWMON range to be from -8dBm to +3dBm • Added the manufacturing data to the vendor specific I2C commands. • Added note about using torque screw-driver for mounting the transponder. • Added Optical Transmit Eye Mask specification from G.693
0.99d	5/16/2003	• Increased max value of 3.3VA current to 3000mA from 2700mA • Decreased max value of 3.3VD current to 2700mA from 3000mA • Corrected the max temperature back to 70C (had been mistakenly changed in going from rev 0.98b to 0.99. • The following I2C commands were changed to "not supported" o 4F/50 EOL in CFG_ALM o 67 Photodiode Temperature Monitor o 68 Modulator Bias Monitor o 69 Read Error Checker Count o 80 EOLALM
0.99e	7/9/2003	• Added explicit spec for DGD maximum of 7.5ps • Added System Optical Return Loss of 24dB • Reduced TXMONK rise/fall time from 200ps to 100ps • Changed I2C Electrical Interface to properly reflect the specs of the ATmega8 processor (DC and AC tables) • Reduced absolute maximum humidity condition to 85% from 90% • Corrected the M->H Vendor Data Write response in section A.3.2.2 • Updated ESD to 25KV Air Discharge test • Added shock, vibration, and fire spread test standards to Quality and Rel section.

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