10GBASE-LRM-LR X2 Transponder

(BBTR10310MS-X1)

PRELIMINARY SPECIFICATIONS – SUBJECT TO CHANGE

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This document provides the specifications for the Big Bear Networks 10GBASE-LRM-LR X2 transponder which meets the IEEE802.3aq D2.2 draft standard for LRM links as well as the IEEE standard for LR links.

Features

- Electro-optical X2 transponder operating at 10.3125 Gb/s
- Supports 10GE LAN PHY (10GBASE-R per Clause 49 of IEEE P802.3ae-2002)
- Hot Pluggable
- Incorporates Big Bear Electronic Dispersion Compensation for robust operation over 300m of installed multimode fiber
- Five diagnostic loop-back modes
- Class I laser
- Compatible with Applicable Industry Standards:
  - XAUI Interface per Clause 47 of IEEE P802.3ae-2002
  - MDIO Interface per Clause 45 of IEEE P802.3ae-2002
  - X2 MSA, Issue 1.0, 2003
  - IEEE802.3aq (Draft 2.2) for LRM links
  - IEEE802.3ae-2002 for LR links

Applications

- Enterprise networks (wiring closet to core)
- LAN networks and Metro Edge

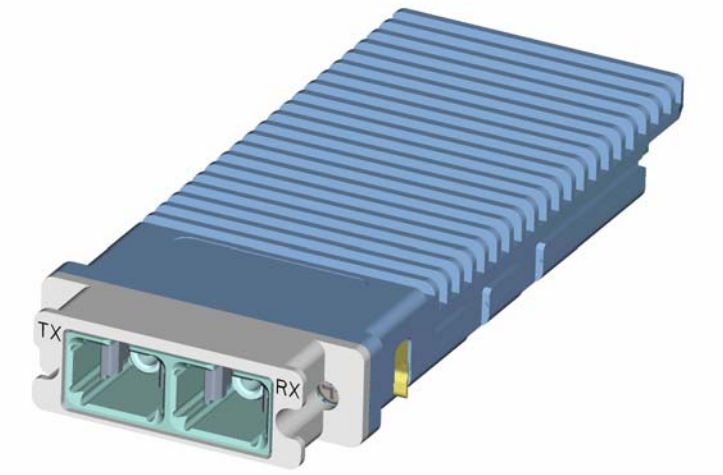

Figure 1: The Big Bear Networks X2 Transponder

NOTE: THE X2 TRANSPONDER IS ALSO AVAILABLE IN THE MID AND TALL HEAT SINK FORMATS

Contents

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General Description

Figure 2 depicts a simplified block diagram of the Big Bear X2 LRM-LR transponder. This bi-directional device provides an electro-optical interface between a serial 10Gb Ethernet optical signal and the XAUI compliant electrical physical layer. The transponder operates the standard 10GbE rate of 10.3125 Gb/s.

A key feature of the BBTR10310MS-X1is its support for both 300m multimode fiber links as well as single mode fiber links of up to 10km or more.

The Big Bear LRM-LR transponder incorporates the latest generation Big Bear Electronic Dispersion Compensation (EDC) which provides compensation for the severe modal dispersion that may occur during propagation through links up to 300m on legacy installed FDDI multimode fiber (see IEEE802.3aq draft for detailed fiber coverage).

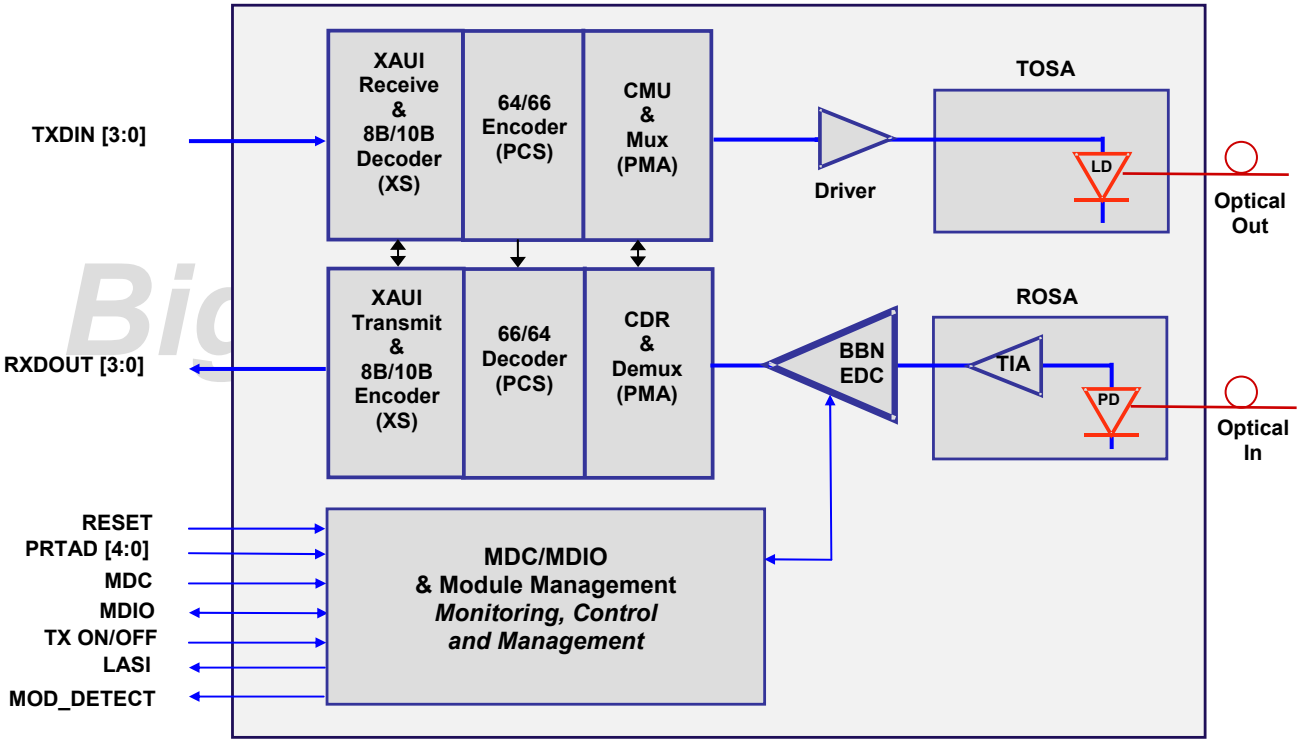

Figure 2: Block Diagram Showing Electrical and Optical Inputs and Outputs

Block Diagram Description

XAUI Interface (Input)

In the optical transmit direction, each 3.125 Gb/s electrical data channel is separately retimed in a clock-and-data recovery block . The retimed data then undergoes Code Alignment and a Lane Deskew before being run through an 8B/10B decoder. The data is rate adjusted then sent through a 64/66B encoder/scrambler, scrambled and finally multiplexed to generate the serial line rate 10.3125 Gb/s electrical signal.

Transmitter

The multiplexed line rate signal at 10.3125 Gb/s is sent through the modulator driver and the resulting amplified signal used to directly drive the 1.3um DFB laser transmitter in the TOSA package.

Receiver

In the receive direction, the transponder accepts a 10.3125Gb/s optical signal and converts this to an electrical signal. The optical receiver of the Big Bear LRM-LR transponder incorporates a large area PIN photodiode and a wide-band trans-impedance amplifier (TIA). This receiver is designed to operate with both multimode fiber and single mode fiber. The raw signal output from the TIA is differentially connected to the electronic dispersion compensation (EDC) device.

Electronic Dispersion Compensation

A key feature of the LRM-LR transponder is the incorporation of the advanced Big Bear electronic dispersion compensation (EDC). The Big Bear EDC device incorporates a Feed Forward Equalizer (FFE) and a Decision Feedback Equalizer (DFE). This architecture provides the high level of compensation required to compensate for the modal dispersion and ISI encountered in legacy FDDI 220m OM1 and OM2 multimode fiber links (300m on OM3). The Big Bear EDC also contains a sophisticated clock recovery architecture for extracting a robust clock from extremely distorted signals.

The Big Bear EDC uses sophisticated adaptive control with rapid tracking time to ensure that the optical link is always tuned for optimal performance.

The DFE block includes the limiting amplifier – ensuring that the slicing decisions are made when the analog eye quality is at its highest level in the receive chain.

XAUI Interface (Output)

Following the EDC the line rate data is sent through the descrambler, 64/66B decoder, 8B/10B encoder, and XAUI serializer. Each XAUI output lane incorporates a transmit equalizer and electrical output driver for optimal signal performance.

MDIO Management Interface

The MDIO interface provides a simple, two wire serial interface to connect a station management entity (STA) and a managed PHY. The management interface consists of the two wire physical interface, a frame format, a protocol specification for exchanging the frames, and a register set that can be read and written using these frames. The two wires of the physical interface are the Management Data Clock (MDC) and the Management Data I/O (MDIO).

A complete list of the supported MDIO registers is given in Appendix A.

Pin Descriptions

Table 1: Data Input and XAUI Interface

Name	I/O	Pins	Type	Description
TXDATA[3:0]_P/N	I	55, 56 58, 59 61, 62 64, 65	Note 1	**Transmit Data.** The Transmit Data (TXDATA[3:0]) signals carry data from the system-side ASIC to the XAUI transceiver
RXDATA[3:0]_P/N	O	41, 42 44, 45 47, 48 50, 51	Note 2	**Receive Data.** The Receive Data (RXDATA[3:0]) signals carry data from XAUI transceiver to the system side ASIC. Per Clause 47 of IEEE P802.3ae-2002 the signal paths are intended to operate up to approximately 50cm over controlled impedance traces on standard FR4 printed circuit boards.
LASI	O	9	1.2V CMOS	**Link Alarm Status Interrupt (LASI)** Logic High = normal operation Logic Low = LASI asserted
RESET	I	10	1.2V CMOS	**Module Reset** Logic High = normal operation Logic Low = Reset Minimum transponder reset assert time is 1ms. (10-22K ohm pull-up in transponder)
TX ON/OFF	I	12	1.2V CMOS	**Transmitter On/Off** Logic High = Transmitter on Logic Low = Transmitter off (Open Drain compatible) (10-22K ohm pull-up in transponder)
MOD DETECT	O	14	NA	**Module Detect.** Indicates presence of the module. Pulled low inside the module through 1K

Note 1: The XAUI Driver lane electrical characteristics follow the specifications given in Clause 47.3.3 of IEEE P802.3ae-2002.

Note 2: The XAUI Receiver lane electrical characteristics follow the specifications given in Clause 47.3.4 of IEEE P802.3ae-2002.

Note 3: A complete pin list is provided in Table 16: Pin-Out List

MDIO Interface

Table 2 MDIO Interface Bus

Name	I/O	Type	Description
MDIO	**I/O**	MDIO (Note 1)	Management Data IO
MDC	**I**	1.2V CMOS (Note 1)	Management Data Clock
PRTAD[4:0]	**I**	1.2V CMOS (Note 1)	5 bit address. Low = 0. [1KOhm pull-down]

Note 1: The transponder adheres to the specification for the MDIO interface in Clause 45 of IEEE P802.3ae-2002.

Module Management

A complete list of the MDIO Registers is provided in Appendix A.

Power and Ground

Table 3: Power & Ground Signals

Name	I/O	*Type*	Description
3.3V	I	Supply	Power supply, +3.3V
5V	I	Supply	Power supply, +5.0V
APS		Supply	Adaptive Power Supply (1.8V in the Big Bear xR MMF Transponder)
APS Sense	O	Analog Signal	Tied to APS power supply rail inside transponder
APS Set	O	Analog Signal	For this transponder the APS supply needs to be 1.5V, therefore the Set Resistor in the transponder is 1Kohm. The APS circuit in the transponder is shown below

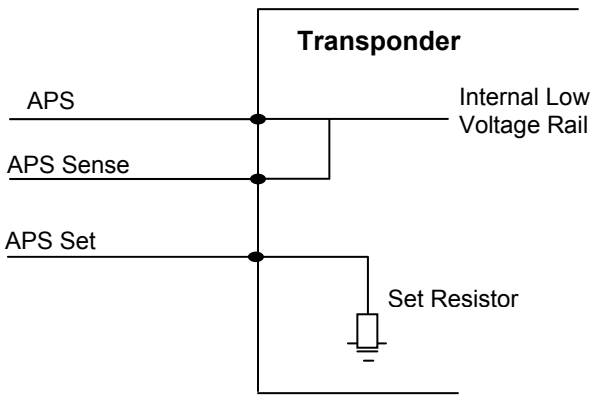

Figure 3 Adaptable Power Supply (APS) Lines

Signal Detect Status Registers

When the received optical power drops below a level of -15 ±1.1 dBm several alarm registers indicate that there is a loss of signal. The affected registers are listed in Table 4 below. The alarm condition is removed when the received optical power rises above -15 ±1.1 dBm. As noted in the table a number of the alarm registers are latching and will only be cleared on a read of that register.

Table 4: Signal Detect Alarm Fault Registers

Parameter	Register	Register state on Loss of Optical Signal	Indicating
Global PMD Receive Signal Detect	1.10.0 (1.0x000A.0)	0	Indicates that signal not detected on receiver. This alarm is non-latching.
PMA/PMD Fault	1.1.7 (1.0x0001.7)	1	Indicates a local fault condition in the PMA/PMD This alarm is non-latching.
PMA/PMD Receive Fault	1.8.10 (1.0x0008.10)	1	Indicates a fault condition on the receive path (This alarm is latches high and is cleared on a read of this register)
Receive Optical Power Fault	1.36867.5 (1.0x9003.5)	1	Receive Optical Power Fault (This alarm is latches high and is cleared on a read of this register)

Note that both the 'Global PMD Receive Signal Detect' and the 'Receive Optical Power Fault' feed into the Link Alarm Status Interrupt.

Link Alarm Status Interrupt

Per the XENPAK MSA the Link Alarm Status Interrupt (LASI) pin is used to indicate a performance issue with either the transmit path or the receive path. LASI is the OR of the TX_ALARM, the RX_ALARM, and the LINK_STATUS ALARM. The components contributing to these alarms are shown in the MDIO register list in Appendix A, specifically 0x9004, 0x9003 for the TX_ALARM and RX_ALARM. (The items contributing to the LINK_STATUS alarm are listed at the end of the LASI section of Appendix A) The functionality of the LASI signal is shown below in Figure 4.

Latching
Most contributing components of the TX_ALARM and RX_ALARM are latching and are cleared only when that bit of the status register is read. The LS_ALARM is latching and is asserted each time the LINK_STATUS signal changes state. LS_ALARM is cleared on a read of the LASI Status Register (1.0x9005).

Enabling and Masking
For the TX_ALARM and the RX_ALARM each of the contributing components can be independently enabled or disabled using the control registers 0x9001 and 0x9003. All three of the net TX, RX and LS alarms can be masked using the control register 0x9002 before the final OR function to produce the LASI signal.

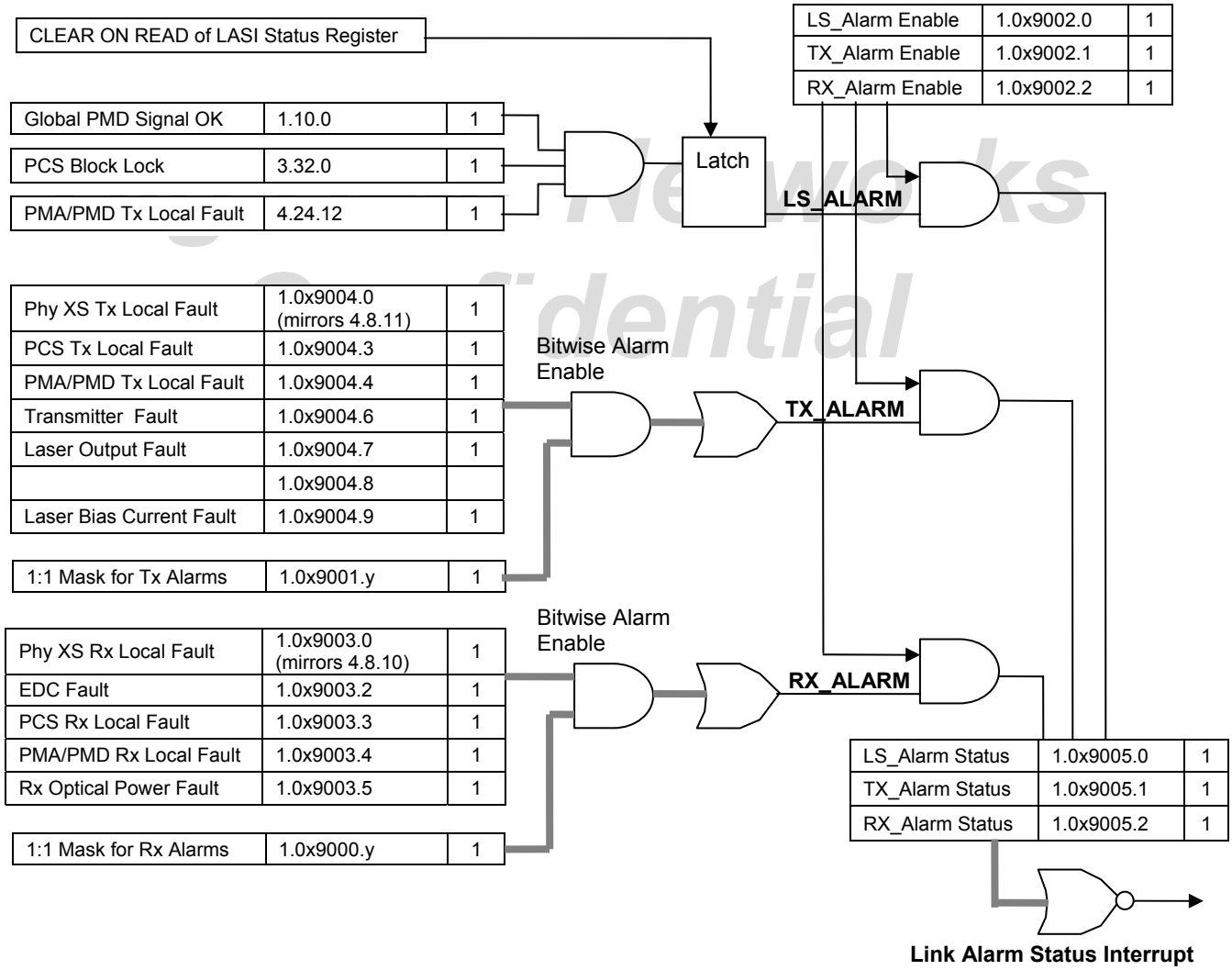

Figure 4: Link Alarm Status Interrupt signal (LASI) Block Diagram

Loop-back Modes

Five loop-back modes are supported in the Big Bear LRM-LR transponder. In a 'System Loop-back' the data on the transmit path is looped back into the receive path (see loops 1 to 3 below for PHY XS, PCS, and PMA system loop-backs). In 'Network Loop-back the data on the receive path is looped back into the transmit path (see loops 4 and 5 below for PHY XS Network Loop-back, and PMA Network Loop-back.)

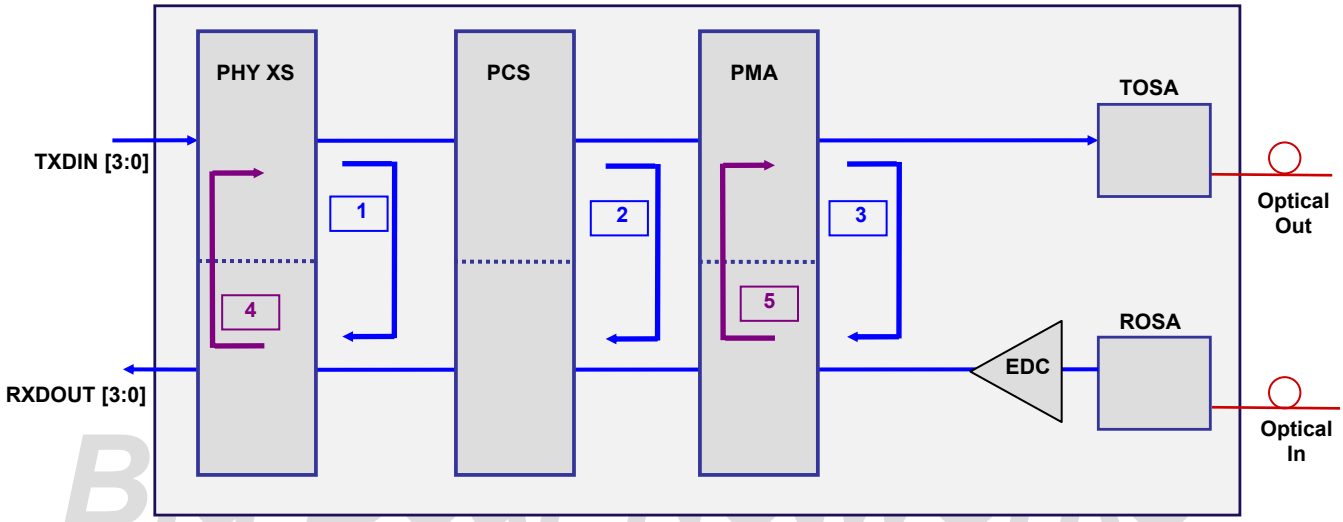

Figure 5: Diagram of Loop-back Modes

Table 5: Loop-back Mode Details

	Loop-back Mode	Control Register	Description	Bypassed Path Default Output	Data Output Enable Register	Bypassed Path Data with Output Enable =1
1	**XGXS System Loopback**	4.49152.14 (4.0xC000.14)	Connects the XAUI 10B/8B Decoder output to the XAUI 8B/10B encoder input.	All 1's at Optical Out	4.49152.15 (4.0xC000.15)	Transmit Data at Optical Out
2	**PCS System Loopback**	3.0.14 (3.0x000.14)	The PCS accepts data on the transmit path from the XGMII and returns it on the receive path to the XCMII. (802.3ae Clause 49.2.14.4)	0x00FF at Optical Out	3.0.5 (3.0x000.5)	Transmit Data at Optical Out
3	**PMA System Loopback**	1.0.0 (1.0x000.0)	When PMA system loop-back is enabled then transmission requests passed to the transmitter are shunted directly to the receiver, overriding any signal detected by the receiver on its attached link. (802.3ae Clause 51.8)	Transmit Data at Optical Out	NA	NA
4	**XGXS Network Loopback**	4.0.14 (4.0x000.14)	After the network data has passed through the 8B/10B encoder it is looped back to the transmit side. Per 802.3ae loopback applies to all lanes as a group with lane 0 on the receive chain looped back to lane 0 on the transmit chain. (Here transmit and receive are defined relative to the optical signal direction). (802.3ae Clause 48.3.3).	Receive Data to RXDOUT	NA	NA
5	**PMA Network Loopback**	1.49153.4 (1.0xC001.4)	PMA Network Loop-back returns the received optical signal immediately following the CDR to provide a retimed, de-jittered signal to the output driver of the Tx.	Receive Data to RXDOUT	1.49153.9 (1.0xC001.9)	Idle at RXDOUT

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 6 Absolute Maximum Ratings

Rating	*Symbol*	*Min*	*Max*	*Units*
Storage Case Temperature	T_{stg}	–40	+85	°C
Receive Average Optical Input Power P_{IN}	P_{MAX}		+4	dBm
+3.3V Supplies		-0.3	+3.6	V
+5.0V Supplies		-0.3	+6.0	V
APS Supplies		-0.3	+1.5	V
LV-CMOS Input Voltage		-0.7	4.0	V
LV-CMOS Output Voltage			2.5	V
Static Discharge Voltage (Human Body Model)	ESD		2000	V
Relative Humidity (non-condensing)	RH	15	90	%

Recommended Operating Conditions

Minimum and maximum values specified over operating case temperature range. Typical values are measured at room temperature unless otherwise noted.

Table 7 Standard Operating Conditions

Parameter	*Name*	*Conditions*	*Min*	*Typical*	*Max*	*Units*
Operating Case Temperature	T_C		0		70	°C
Transponder Power Consumption	P_{DIS}				4	W
+3.3V Power Supply Voltage	+3.3V		3.135	3.3	3.465	V
+5.0V Power Supply Voltage	+5.0V		4.75	5.0	5.25	V
APS Power Supply Voltage	APS	Note 1.	1.21	1.25	1.29	V
+3.3V Power Supply Current	3.3V				1200	mA
+5.0V Power Supply Current	5.0V				0	mA
APS Power Supply Current	APS				1000	mA
Ripple and Noise					40	mV rms

Note 1: Required APS supply range is ± 3%

Hot Swapping

The module can be hot-swapped.

Table 8 Turn-On Characteristics

Parameter	*Name*	*Conditions*	*Min*	*Typical*	*Max*	*Units*
Peak Inrush Current	I_{CC} Peak				0.75	A / pin
Current Ramp Rate (for I < 100mA)	dI_{CC}/dt				50	mA/ms
Current Ramp Rate (for I > 100mA)	dI_{CC}/dt	*Note 1*			100	mA/ms
Initialization Time	T_{INIT}			TBD	5	Seconds

Note 1: Current step of 90mA during module initialization.

Optical Characteristics

The Big Bear LRM-LR transponder meets the IEEE802.3aq D2.2 draft standard for LRM links and the IEEE standard for single mode 10km LR links.

The optical specifications are split into three groups:

1. Specifications common to LRM and LR which are either the same or where the worst case value is used.
2. Specifications pertaining to LRM performance only
3. Specifications pertaining to LR performance only.

All specifications are End Of Life.

Table 9: LRM-LR Transponder Optical Characteristics (Common to LRM and LR)

Parameter	*Symbol*	*Conditions*	*Min*	*Typical*	*Max*	*Units*
Transmitter						
Center Wavelength	λ_C		1260		1355	nm
Average Launch Power	P_O	(Note 1) (Note 2)	-6.5		+0.5	dBm
Average Launch Power OFF					-30	dBm
Launch Power OMA		(Note 3)	-4.5		+1.5	dBm
Extinction Ratio	ER		3.5			dB
RIN OMA					-128	dBOMA/Hz
Optical Return Loss Tolerance					12	dB
Transmitter Reflectance					-12	dB
Eye Mask Margin			0			%
Transmitter Eye Mask {X1, X2, X3, Y1, Y2, Y3}		(Note 4) See Figure 6	{0.25, 0.40, 0.45, 0.25, 0.28, 0.40}			
Receiver						
Nominal Center Wavelength	λ_{NOM}		1260		1355	nm
Max Average Receive Power		*(Note 5)*			*0.5*	*dBm*
Receiver Reflectance					-12	dB

Notes:

1. Average Output Power (min) is informative only – a transmitter with power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. The IEEE802.3aq D2.2 Minimum average launch power specification for LRM is the more restrictive and is the one used.
3. The IEEE802.3aq D2.2 Minimum launch power OMA for LRM is the more restrictive and is the one used. There is no max launch OMA specification for LR so the LRM value is used.
4. The transmit eye mask of the LR standard is more restrictive and is the one used (200 waveforms).
5. Maximum Average Receive Power is informative only.

Table 10: LRM Specific Optical Characteristics

Parameter	*Symbol*	*Conditions*	*Min*	*Typical*	*Max*	*Units*
Transmitter						
RMS Spectral Width at 1260nm					2.4	nm
RMS Spectral Width at 1300nm and 1355nm					4	nm
TWDP		(Note 1)			4.7	dB
Uncorrelated Jitter					0.033	UI
Encircled Flux in 5 micron radius		(Note 2)			30	%
Encircled Flux in 11 micron radius		(Note 2)			86	%
Receiver						
Overload Received Power (OMA)					1.5	dBm
Min Received Power (OMA)		(Note 3)	*-6.5*			*dBm*
Comprehensive Stressed Receiver Sensitivity		(Note 4)			-6.5	dBm
Simple Stressed Receiver Sensitivity OMA		*(Note 5)*			*-7.5*	*dBm*
Jitter tolerance at 40KHz (p-p)			5			UI
Min Average receive power		*(Note 6)*	*-8.5*			*dBm*

Notes:

1. TWDP: Transmitter waveform and dispersion penalty. See IEEE802.3aq draft 2.2 for complete definition.
2. See IEEE802.3aq D2.2 Table 68-3? for detail of encircled flux specification
3. The Min Received Power (OMA) is informative only.
4. See Table 68.4? in the IEEE802.3aq D2.2 for details of the comprehensive stressed tests for TP3.
5. This test is informative only. See IEEE802.3aq D2.2 for detail on the simple stressed receiver sensitivity.
6. Minimum Average Receive Power is informative only – a received power below this value cannot be compliant; however, a value above this does not ensure compliance.

Table 11: LR Specific Optical Characteristics

Parameter	*Symbol*	*Conditions*	*Min*	*Typical*	*Max*	*Units*
Transmitter						
Side Mode Suppression Ratio					30	dB
Transmitter Dispersion Penalty					3.2	dB
Launch OMA – TDP					-6.2	dBm
Receiver						
Stressed Receiver Sensitivity (OMA)		(Note 1)			-10.3	dBm
Max Receiver Sensitivity (OMA)		*(Note 2)*			*-12.6*	*dBm*
Stressed Eye Jitter			0.3			UI
Min Average receive power		*(Note 3)*	*-14.4*			*dBm*
Vertical Eye Closure Penalty			2.2			dB
Receive 3dB upper cut off freq.					12.3	GHz

Notes:

1. See Section 52.9.9.2 in the IEEE802.3ae for details of the LR stressed tests for TP3.
2. This is for the back-to-back condition and is informative only.
3. Minimum Average Receive Power is informative only – a received power below this value cannot be compliant; however, a value above this does not ensure compliance.

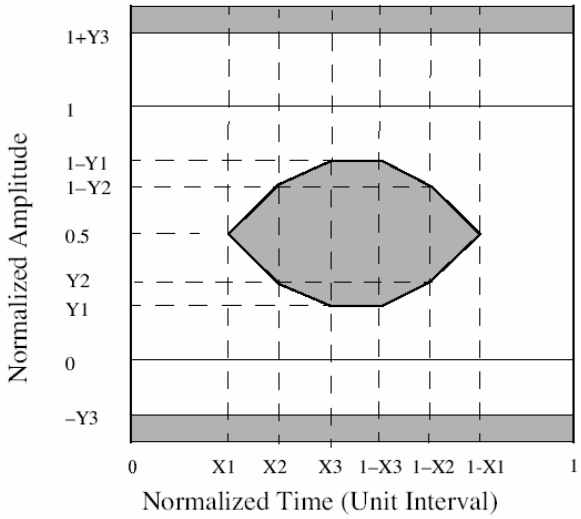

Figure 6: Transmitter Eye Mask Definition (Per IEEE802.3ae sect 52.9.7)

Electrical Characteristics

A X2 module will be functionally operational within 5 seconds of insertion. Parametric performance (such as laser line-width) may depend on thermal stabilization of the module and may take substantially longer and will depend on the thermal environment imposed by the host.

The XAUI electrical interface on the Big Bear Transponder complies fully with Clause 47 of IEEE802.3ae-2002.

Table 12: XAUI Input Interface

Parameter	*Symbol*	*Conditions*	*Min*	*Typical*	*Max*	*Units*
Input Differential Voltage	$V_{IN\ DIFF}$	p-p swing (Note 1)	160		1600	mV
Differential Input Impedance	$Z_{IN\ DIFF}$		80		120	Ω
Jitter tolerance		(Note 2)				

Notes
1. The XAUI receiver successfully handles signals that meet the far-end eye mask per Section 47.3.3.5 of IEEE P802.3ae-2002.
2. The XAUI receiver meets sinusoidal jitter tolerance mask in figure 47-5 of IEEE P802.3ae-2002

Table 13: XAUI Driver Interface

Parameter	*Symbol*	*Conditions*	*Min*	*Typical*	*Max*	*Units*
Output Differential Voltage	$V_{OUT\ DIFF}$	p-p swing (Note 1)	800		1600	mV
Differential Output Impedance	$Z_{OUT\ DIFF}$		80		120	Ω
Rise and Fall times	Tr, Tf		40		100	ps
Total Transmit Jitter		No Pre-equalization at near end			0.35	UI

Notes
1. The XAUI driver meets the near or far eye mask per Section 47.3.3.5 of IEEE P802.3ae-2002.

Table 14 LV-CMOS Input and Output Characteristics

Parameter	*Symbol*	*Conditions*	*Min*	*Typical*	*Max*	*Units*
LV-CMOS Input DC Characteristics						
Input High Voltage	V_{IH}		0.84		*Note 1*	V
Input Low Voltage	V_{IL}				0.36	V
Input Pulldown Current	I_{PD}	V_{IN}=1.2V	20	40	120	µA
LV-CMOS Output DC Characteristics						
Output High Voltage	V_{OH}	I_{OH}=-4mA	1.0		1.5	V
Output Low Voltage	V_{OL}	I_{OL}= 4mA			0.15	V
LV-CMOS AC Characteristics						
Rise Time	T_{RISE}	C_{LOAD} = 300pF			30	µs
Fall Time	T_{FALL}	C_{LOAD} = 300pF			50	ns

Notes
1. Nominally 1.5V, but 3.3V Tolerant

Table 15 MDIO Input and Output Characteristics

Parameter	*Symbol*	*Conditions*	*Min*	*Typical*	*Max*	*Units*
MDIO Input DC Characteristics						
Input High Voltage	V_{IH}		0.84		1.5	V
Input Low Voltage	V_{IL}		-0.3		0.36	V
MDIO Output DC Characteristics						
Output High Voltage	V_{OH}	I_{OH}=-100 uA	1.0		1.5	V
Output Low Voltage	V_{OL}	I_{OL}= 100 uA	-0.3		0.2	V
Output High Current	I_{OL}	V_{IN}=0.3V	-4			mA
MDIO AC Characteristics						
Input Capacitance	Ci				10	pF
MDIO Data Hold Time	T_{hold}		10			ns
MDIO Data Setup Time	T_{setup}		10			ns
Delay (MDC rising edge to MDIO data change)	Tdelay				300	ns
MDC Clock Rate					2.5	Mb/s

Electrical Connector

The X2 transponder PCB forms the male half of the 70-way two row electrical connector and is designed to mate with TycoAMP Part 1367337-1 or Molex Part 74441-0003 or equivalent. The pin numbering and orientation on the transponder PCB are shown below in Figure 7.

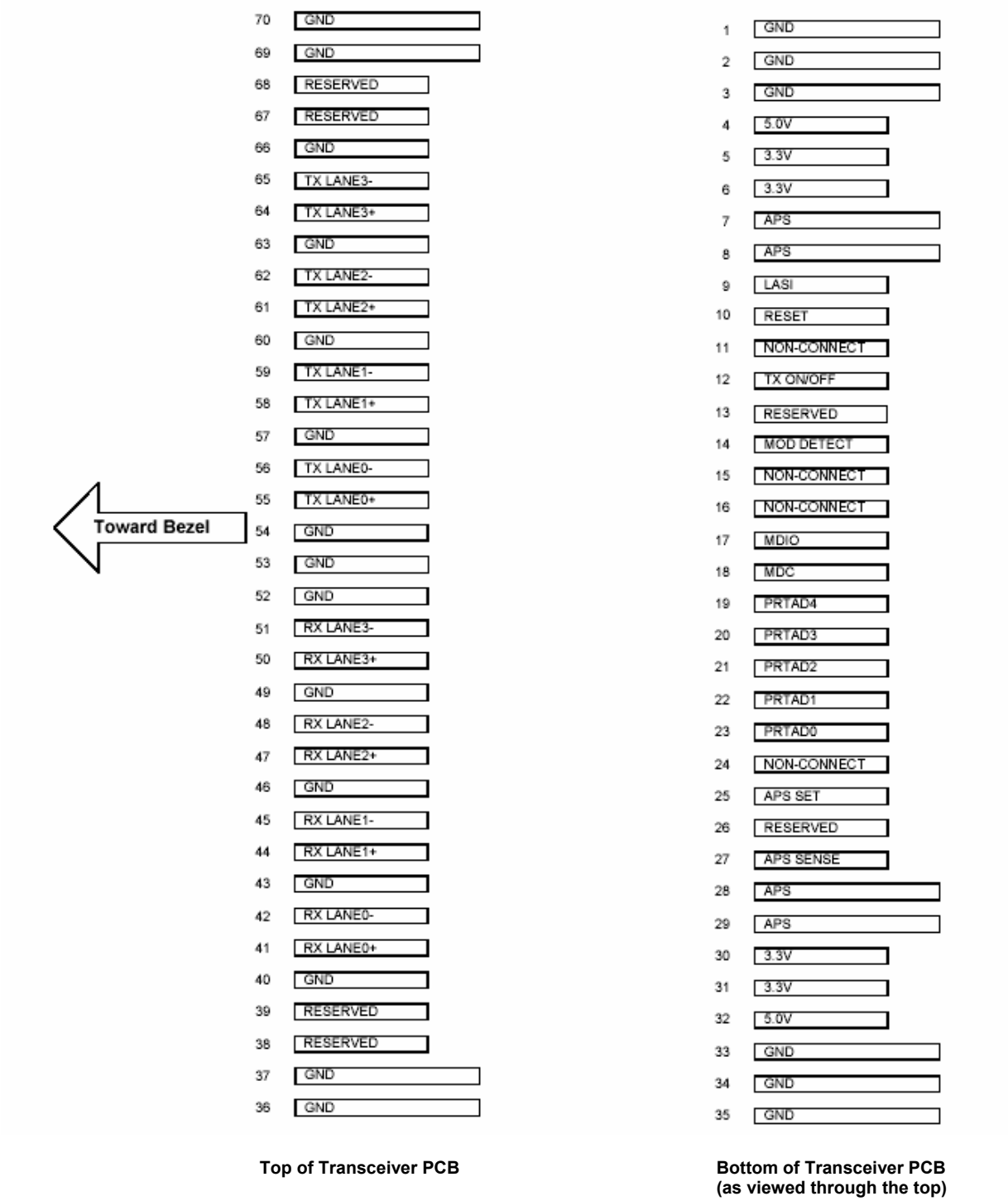

Figure 7: Electrical Connection Pad Layout

Electrical Pin-Out List

The pin function definitions are provided in below. Note that pins 1-35 are constitute the lower row, while pins 36 -70 constitute the upper row.

Table 16: Pin-Out List

Pin #	Name	Dir	Function	Note
1	GND		Electrical Ground	
2	GND		Electrical Ground	
3	GND		Electrical Ground	
4	5V	I	Power	
5	3.3V	I	Power	
6	3.3V	I	Power	
7	APS	I	Adaptive Power Supply (1.25V)	
8	APS	I	Adaptive Power Supply (1.25V)	
9	LASI	O	Link Alarm Status Interrupt High = Normal Operation Low = LASI asserted 10K ohm pull-up on transponder.	
10	RESET	I	Module Reset High = Normal Operation Low = Reset	
11	NOT CONNECTED			
12	Tx On/Off	I	High = Transmitter On Low = Transmitter Off 10K ohm pull-up on transponder.	
13	NOT CONNECTED			
14	MOD DETECT	O	Pulled low inside transponder through 1K Ohm	
15	NOT CONNECTED			
16	NOT CONNECTED			
17	MDIO	I/O	Management Data I/O	
18	MDC	I	Management Data Clock	
19	PRTAD4	I	Port Address Bit 4	
20	PRTAD3	I	Port Address Bit 3	
21	PRTAD2	I	Port Address Bit 2	
22	PRTAD1	I	Port Address Bit 1	
23	PRTAD0	I	Port Address Bit 0	
24	NOT CONNECTED	I		
25	APS SET	I	Feedback input for APS	
26	RESERVED		Reserved for APD use	
27	APS SENSE	I	APS Sense Connection	
28	APS	I	Adaptive Power Supply (1.25V)	
29	APS	I	Adaptive Power Supply (1.25V)	
30	3.3V	I	Power	
3	3.3V	I	Power	

32	5.0V	I	Power	
33	GND		Electrical Ground	
34	GND		Electrical Ground	
35	GND		Electrical Ground	
36	GND		Electrical Ground	
37	GND		Electrical Ground	
38	RESERVED			
39	RESERVED			
40	GND		Electrical Ground	
41	RX LANE 0+	O	Module XAUI Output Lane 0+	
42	RX LANE 0-	O	Module XAUI Output Lane 0-	
43	GND		Electrical Ground	
44	RX LANE 1+	O	Module XAUI Output Lane 1+	
45	RX LANE 1-	O	Module XAUI Output Lane 1-	
46	GND		Electrical Ground	
47	RX LANE 2+	O	Module XAUI Output Lane 2+	
48	RX LANE 2-	O	Module XAUI Output Lane 2-	
49	GND		Electrical Ground	
50	RX LANE 3+	O	Module XAUI Output Lane 3+	
51	RX LANE 3-	O	Module XAUI Output Lane 3-	
52	GND		Electrical Ground	
53	GND		Electrical Ground	
54	GND		Electrical Ground	
55	TX LANE 0+	O	Module XAUI Input Lane 0+	
56	TX LANE 0-	O	Module XAUI Input Lane 0-	
57	GND		Electrical Ground	
58	TX LANE 1+	O	Module XAUI Input Lane 1+	
59	TX LANE 1-	O	Module XAUI Input Lane 1-	
60	GND		Electrical Ground	
61	TX LANE 2+	O	Module XAUI Input Lane 2+	
62	TX LANE 2-	O	Module XAUI Input Lane 2-	
63	GND		Electrical Ground	
64	TX LANE 3+	O	Module XAUI Input Lane 3+	
65	TX LANE 3-	O	Module XAUI Input Lane 3-	
66	GND		Electrical Ground	
67	RESERVED			
68	RESERVED			
69	GND		Electrical Ground	
70	GND		Electrical Ground	

Package Outline Diagram

Table 17 Mechanical Dimensions

Parameter	*Notes*	*Value (inches)*	*Value (mm)*
A	Note 1		39.6
B	Note 1		12.0
C	Note 1		11.0
Type of electrical interface		XAUI	
Type of optical interface	Note 2	SC Duplex Receptacle	

Note 1: Mechanical dimensions conform to Section 6.8 of X2 MSA Rev 1.0
Note 2: Per section 6.16 of X2 MSA Rev 1.0

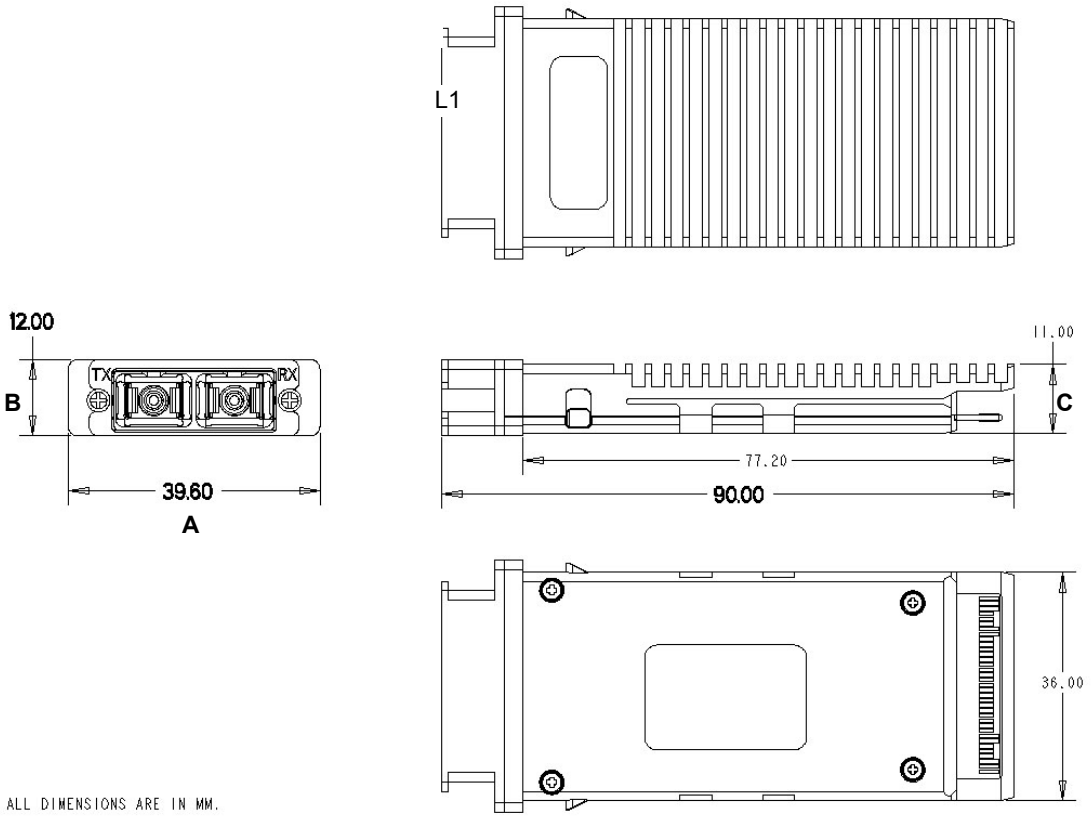

Figure 8 Transponder Mechanical Drawing

NOTE: THE X2 TRANSPONDER IS ALSO AVAILABLE IN THE MID AND TALL HEAT SINK FORMATS

Safety

The transponder is classified as a Class I laser product per IEC 60825-1 and pre CFR 21 part 1040.10

Reliability and Qualification

To ensure high product reliability and customer satisfaction, Big Bear Networks has developed a comprehensive Quality and Reliability program. All Transponders are qualified to Big Bear Networks internal standards using MIL-STD-883 test methods and procedures and sampling techniques consistent with Telcordia Technologies requirements. This program characterizes and qualifies components and products starting at the design phase, and on-going through the manufacturing process. The qualification test requirements are designed based on the following industry standards:

- Transponders subassemblies based on GR-468 (opto-electronic devices)

Contact Big Bear Networks for the latest information on our product qualification plans and reliability specifications.

References

The following references are provided for informational purposes only. The parameters and operational behavior outlined in this specification describe the complete functionality of the 10G Transponder. Contact Big Bear Networks for any items concerning the operational characteristics of this device.

1. IEEE 802.3ae-2002, August 30, 2002.
2. Draft IEEE 802.3aq D2.2 , August 2005
3. XENPAK MSA Rev 3.0, September 18, 2002.
4. X2 MSA Rev 1.0, January 30, 2003.

Appendix A: MDIO Registers

The transponder adheres to the general specification for the MDIO interface given in Clause 45 of IEEE P802.3ae-2002.

Note that the MDIO register functionality is taken from the following source documents:

- PMA/PMD Registers 0x0000 to 0x000F are taken from IEEE802.3ae section 45.2.1
- PMA/PMD Registers 0x8000 to 0x8FFF are taken from XENPAK MSA 3.0 section 10.8 – 10.12
- The LASI Section 0x9000 to 0x9005 is taken from XENPAK MSA 3.0 section 10.13
- PCS Registers 0x0000 to 0xFFFF are taken from IEEE802.3ae section 45.2.3
- PHY XS Registers 0x0000 to 0xFFFF are taken from IEEE802.3ae section 45.2.4

Device 1 PMA/PMD Registers

Device	PMA/PMD Register (Decimal)	PMA/PMD Register (Hex)	Register Name
1	0		PMA/PMD Control 1
1	1		PMA/PMD Status 1
1	2-3		Device Identifier
1	4		PMA/PMD Speed Ability
1	5-6		Devices in Package
1	7		10G PMA/PMD Control 2
1	8		10G PMA/PMD Status 2
1	9		10G PMD transmit disable
1	10		10G PMD receive signal detect
1	14-15		Package Identifier
1	32768	8000	NVR Control/Status
1	32775	8007	XENPAK MSA supported
1	32776-32777	8008 - 8009	NVR size in bytes
1	32778-32778	800A-800B	Number of bytes used
1	32780	800C	Basic Field Address
1	32781	800D	Customer Field Address
1	32782	800E	Vendor Field Address
1	32783 - 32784	800F-8010	Extended Vendor Field Address
1	32785	8011	Reserved
1	32786	8012	Transceiver Type
1	32787	8013	Optical Connector Type
1	32787	8014	Bit Encoding
1	32789-32790	8015 - 8016	Nominal Bit Rate (in multiples of 1Mb/s)
1	32791	8017	Protocol Type

Device	PMA/PMD Register (Decimal)	PMA/PMD Register (Hex)	Register Name
1	32792-32801	8018 - 8021	Standards Compliance Codes 10GbE Code Byte 0
1	32802-32803	8022 – 8023	Specified Transmission Range (In 10m Increments)
1	32804-32805	8024 – 8025	Fiber type Byte 0 and Byte 1
1	32806 - 32808	8026 – 8028	Center Optical Wavelength(in 0.01nm steps - Channel 0)
1	32818 - 32821	8032 - 8035	Package Identifier OUI
1	32822-32825	8036 - 8039	Transceiver Vendor OUI
1	32826-32841	803A – 8049	Transceiver Vendor name in ASCII
1	32842-32875	804A – 8059	Part number provided by Transceiver vendor in ASCII
1	32858-32859	805A – 805B	Revision level for part - provided by Vendor (ASCII)
1	32860-32875	805C – 806B	Vendor Serial Number in ASCII
1	32876-32885	806C - 8075	Vendor manufacturing date code in ASCII
1	32886	8076	5V stressed environmental reference
1	32887	8077	3.3V stressed environmental reference
1	32888	8078	APS stressed environment reference
1	32889	8079	Nominal APS voltage
1	32890	807A	DOM Capability
1	32891	807B	Reserved
1	32893	807D	Basic Field Checksum
1	32894-32941	807E – 80AD	Customer writable area
1	32942-33030	80AE – 8106	Vendor Specific
1	33031-36863	8107 – 8FFF	Extended Vendor Specific
1	36864	9000	RX_ALARM Control
1	36865	9001	TX_ALARM Control
1	36866	9002	LASI Control
1	36867	9003	RX_ALARM Status
1	36868	9004	TX_ALARM Status
1	36869	9005	LASI Status
1	49153	C001	Extended PMA Features
1	49155	C003	PMA/PMD Vendor Specific
1	49156	C004	PMA/PMD Vendor Specific Checksum
1	49188	C024	PMA Vendor Specific

Register 1.0 (0x0000) – PMA/PMD Control

Bit	Name	Description	R/W	Default
1.0.15	Reset	1= PMA/PMD reset 0 = normal operation Sets all PMA/PMD registers to their default states.	RW	0
1.0.14	Reserved	Value always 0, writes ignored	RW	0
1.0.13	Speed Selection	1= Operation at 10Gb/s and above 0 = Unspecified NOTE 1	RW	1
1.0.12	Reserved	Value always 0, writes ignored	RW	0
1.0.11	Low Power	1 = Low power mode 0 = Normal operation	RW	0
1.0.10:7	Reserved	Value always 0, writes ignored	RW	0
1.0.6	Speed Selection	1 = Operation at 10Gb/s and above 0 = Unspecified NOTE 1	RW	1
1.0.5:2	Speed Selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = Reserved 0 0 0 0 = 10Gb/s	RW	0 0 0 0
1.0.1	Reserved	Value always 0, writes ignored	RW	0
1.0.0	PMA Loopback	1=Enable PMA loopback 0=Disable PMA loopback	RW	0

Note 1: Bits 6 and 13 both need to be set to '1'. These locations were previously used by Clause 22 to set the speed of devices running at speeds of 1Gb/s and below.

Register 1.1 (0x0001) – PMA/PMD Status 1

Bit	Name	Description	R/W	Default
1.1.15:8	Reserved	NA	RO	NA
1.1.7	Fault	1 = Local fault condition detected in PMA/PMD 0 = Local fault condition not detected in PMA/PMD Alarm = TX Local Fault or RX Local Fault (i.e. when either 1.8.11 or 1.8.10 are set high)	RO	0
1.1.6:3	Reserved	NA	RO/LL	NA
1.1.2	Receive Link Status	1 = PMA locked to receive signal 0 = PMA not locked to receive signal	RO/LL	1
1.1.1	Power down ability	1 = PMA/PMD supports low power mode 0 = PMA/PMD does not support low power mode	RO	??
1.1.0	Reserved	NA		NA

Register 1.2 to 1.3 (0x0002 – 0x0003) – Device Identifier

Bit	Name	Description	R/W	Default
1.3.15:0	PMA Identifier		RO	
1.2.15:0	PMA Identifier		RO	

These registers enable the provision of a unique identifier for a particular type of PMA/PMD – see IEEE802.3ae for further detail. Currently Big Bear fills these registers with all zero bits.

Register 1.4 (0x0004) – PMA/PMD Speed Ability

Bit	Name	Description	R/W	Default
1.4.15:1	Reserved (future)		RO	0
1.4.0	10G Capable	1 = PMA/PMD is capable of operating at 10Gb/s 0 = PMA/PMD is not capable of operating at 10Gb/s	RO	1

Register 1.5 to 1.6 (0x0005 – 0x0006) – PMA/PMD Devices in Package

Bit	Name	Description	R/W	Default
1.6.15	Vendor Specific Device 2 present	1 = Vendor specific device 2 present 0 = Vendor specific device 2 not present in package	RO	0
1.6.14	Vendor Specific Device 1 present	1 = Vendor specific device 1 present 0 = Vendor specific device 1 not present in package	RO	1
1.6.13:0	Reserved	N/A	RO	
1.5.15:6	Reserved	N/A	RO	
1.5.5	DTE XS Present	1 = DTE XS present in package 0 = DTE XS not present in package	RO	0
1.5.4	PHY XS Present	1 = PHY XS present in package 0 = PHY XS not present in package	RO	1
1.5.3	PCS Present	1 = PCS present in package 0 = PCS not present in package	RO	1
1.5.2	WIS Present	1 = WIS present in package 0 = WIS not present in package	RO	0
1.5.1	PMA/PMD Present	1 = PMA/PMD present in package 0 = PMA/PMD not present in package	RO	1
1.5.0	Clause 22 Registers present	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	RO	0

Register 1.7 (0x0007) – 10G PMA/PMD Control 2

Bit	Name	Description	R/W	Default
1.7.15:4	Reserved	Value always 0, writes ignored	R/W	0
1.7.3:0	PMA/PMD type selection	3 2 1 0 1 1 X X Reserved 1 0 1 X Reserved 1 0 0 0 10GBASE-LRM 0 1 1 1 10GBASE-SR PMA/PMD type 0 1 1 0 10GBASE-LR PMA/PMD type 0 1 0 1 10GBASE-ER PMA/PMD type 0 1 0 0 10GBASE-LX4 PMA/PMD type 0 0 1 1 10GBASE-SW PMA/PMD type 0 0 1 0 10GBASE-LW PMA/PMD type 0 0 0 1 10GBASE-EW PMA/PMD type 0 0 0 0 10GBASE-CX4 PMA/PMD type	R/W	1000

Register 1.8 (0x0008) – 10G PMA/PMD Status 2

Bit	Name	Description	R/W	Default
1.8.15:14	Device Present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO	10
1.8.13	Transmit fault ability	1 = PMA/PMD has the ability to detect a fault condition on the transmit path 0 = PMA/PMD does not have the ability to detect a fault condition on the transmit path	RO	1
1.8.12	Receive Fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path	RO	1
1.8.11	Transmit Fault	1 = Fault condition on the transmit path 0 = No Fault condition on the transmit path Transmit Fault = Tx PLL loss of lock + Laser Bias Alarm + Laser Output Power Alarm	RO/LH	0
1.8.10	Receive Fault	1 = Fault condition on the receive path 0 = No Fault condition on the receive path Receive Fault = RXLoS + Rx PLL loss of lock + EDC PLL loss of lock.	RO/LH	0
1.8.9	Reserved	Ignore on read		
1.8.8	PMD transmit disable ability	1 = PMD has the ability to disable the transmit path 0 = PMD does not have the ability to disable the transmit path	RO	1
1.8.7	10GBASE-SR Ability	1 = PMA/PMD is able to perform 10GBASE –SR 0 = PMA/PMD is not able to performe 10GBASE-SR	RO	0
1.8.6	10GBASE-LR Ability	1 = PMA/PMD is able to perform 10GBASE –LR 0 = PMA/PMD is not able to performe 10GBASE-LR	RO	1
1.8.5	10GBASE-ER Ability	1 = PMA/PMD is able to perform 10GBASE –ER 0 = PMA/PMD is not able to performe 10GBASE-ER	RO	0
1.8.4	10GBASE-LX4 Ability	1 = PMA/PMD is able to perform 10GBASE –LX4 0 = PMA/PMD is not able to performe 10GBASE-LX4	RO	0
1.8.3	10GBASE-SW Ability	1 = PMA/PMD is able to perform 10GBASE –SW 0 = PMA/PMD is not able to performe 10GBASE-SW	RO	0
1.8.2	10GBASE-LW Ability	1 = PMA/PMD is able to perform 10GBASE –LW 0 = PMA/PMD is not able to performe 10GBASE-LW	RO	0
1.8.1	10GBASE-EW Ability	1 = PMA/PMD is able to perform 10GBASE –EW 0 = PMA/PMD is not able to performe 10GBASE-EW	RO	0
1.8.0	PMA Loopback ability	1 = PMA has the ability to perform a loopback function 0 = PMA does not have the ability to perform a loopback function	RO	1

Register 1.9 (0x0009) – 10G PMD Transmit Disable

Bit	Name	Description	R/W	Default
1.9.15:5	Reserved	Value always 0, writes ignored	R/W	0
1.9.4:1	Not Used	(Used for LX4 Only)	R/W	0
1.9.0	Global PMD Transmit Disable	1 = Disable transmitter output 0 = Enable transmitter output	R/W	0

Register 1.10 (0x000A) – 10G PMD Receive Signal Detect

Bit	Name	Description	R/W	Default
1.10.15:5	Reserved	Value always 0, writes ignored	RO	0
1.10.4:1	Not Used	(Used for LX4 Only)	RO	0
1.10.0	Global PMD receive signal detect	1 = Signal detected on receiver 0 = Signal not detected on receiver Alarm = RX LoS < -15 ±1.1 dBm	RO	1

Register 1.11 (0x000B) – 10G PMA/PMD Extended Ability register bit definitions

Bit	Name	Description	R/W	Default
1.11.15:3	Reserved	Ignore on Read	RO	
1.11.1	10GBASE-LRM Ability	1 = PMA/PMD is able to perform 10GBASE-LRM 0 = PMA/PMD is not able to perform 10GBASE-LRM	RO	0 (Note 1)
1.11.0	10GBASE-CX4 Ability	1 = PMA/PMD is able to perform 10GBASE-CX4 0 = PMA/PMD is not able to perform 10GBASE-CX4	RO	0

Note 1: The current PMA does not support this new register at this point in time and will return a 0 in this field.

Registers 1.14 – 1.15 (0x000E-0x000F) – PMA/PMD package identifier

Registers 1.14 and 1.15 provide a 32 bit value, which may constitute a unique identifier for a particular type of package that the PMA/PMD is instantiated with. The identifier shall be composed of the third through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six bit model number, plus a four-bit revision number.

NOTE that these two registers completely duplicate the values in registers 1.8032h thru 1.8035h and the mapping is shown here.

Bit	Name	Value		Bit	Name	Value
1.15.15	Package Identifier	1.8032h.7		1.14.15	Package Identifier	1.8034h.7
1.15.14	Package Identifier	1.8032h.6		1.14.14	Package Identifier	1.8034h.6
1.15.13	Package Identifier	1.8032h.5		1.14.13	Package Identifier	1.8034h.5
1.15.12	Package Identifier	1.8032h.4		1.14.12	Package Identifier	1.8034h.4
1.15.11	Package Identifier	1.8032h.3		1.14:11	Package Identifier	1.8034h.3
1.15.10	Package Identifier	1.8032h.2		1.14:10	NVR Address	1.8034h.2
1.15:9	Package Identifier	1.8032h.1		1.14:9	NVR Address	1.8034h.1
1.15:8	Package Identifier	1.8032h.0		1.14.8	NVR Address	1.8034h.0
1.15.7	Package Identifier	1.8033h.7		1.14.7	NVR Address	1.8035h.7
1.15.6	Package Identifier	1.8033h.6		1.14.6	NVR Address	1.8035h.6
1.15.5	Package Identifier	1.8033h.5		1.14.5	NVR Address	1.8035h.5
1.15.4	Package Identifier	1.8033h.4		1.14.4	Revision Number	1.8035h.4
1.15.3	Package Identifier	1.8033h.3		1.14.3	Revision Number	1.8035h.3
1.15.2	Package Identifier	1.8033h.2		1.14.2	Revision Number	1.8035h.2
1.15.1	Package Identifier	1.8033h.1		1.14.1	Revision Number	1.8035h.1
1.15.0	Package Identifier	1.8033h.0		1.14.0	Reserved	1.8035h.0

NVRAM (0x8000 Series)

Register 1.32768 (0x8000) - NRV Control / Status

Bit	Name	Description	R/W	Default
1.32768.15:9	Vendor Specific	*Will be used for control and status of the Electronic Dispersion Compensation – details TBD*	RW	
1.32768.8:6	Reserved		RO	
1.32768.5	Command	0 = read NVR 1 = write NVR	RW	
1.36864.4	Reserved		RO	
1.36864.3:2	Command Status	00 = Idle 01 = Command completed successfully 10 = Command in progress / queued 11 = Command failed	RO	
1.36864.1:0	Extended Commands	00 = Vendor Specific 01 = Vendor Specific 10 = read/write one byte 11 = read/write all NVR contents	RW	

A summary of the NVRAM settings is provided in descriptions of the NVRAM registers is provided in Table 18 below. More complete descri

Table 18: NVRAM Registers

Register (Hex)	7	6	5	4	3	2	1	0	Comment
8007	0	0	0	1	1	1	1	0	MSA 3.0
8008	0	0	0	0	0	0	0	1	NVR Size is 256 Bytes
8009	0	0	0	0	0	0	0	0	
800A	0	0	0	0	0	0	0	1	Number of Bytes used in the NVR – BBN currently specifies 256
800B	0	0	0	0	0	0	0	0	
800C	0	0	0	0	1	0	1	1	NVR start address is Decimal 11
800D	0	1	1	1	0	1	1	1	Customer Field start address is Decimal 119
800E	1	0	1	0	0	1	1	1	Vendor Field start address is Decimal 167
800F	0	0	0	0	0	0	0	1	Extended Vendor Field start address is Decimal 256
8010	0	0	0	0	0	0	0	0	
8011	0	0	0	0	0	0	0	0	Reserved
8012	0	0	0	0	0	0	1	0	Transponder type is X2
8013	0	0	0	0	0	0	0	1	Optical connector is SC-Duplex
8014	0	0	0	0	0	0	0	1	Encoding is NRZ
8015	0	0	1	0	1	0	0	0	Bit Rate is 10.3125Gb/s
8016	0	1	0	0	1	0	0	0	
8017	0	0	0	0	0	0	0	1	Protocol is 10GbE
8018	0	0	0	0	0	0	0	0	Standards compliance is not specified in XENPAK MSA for LRM-LR (so put all zeros for the moment)
8019	0	0	0	0	0	0	0	0	
801A	0	0	0	0	0	0	0	0	
801B	0	0	0	0	0	0	0	0	
801C	0	0	0	0	0	0	0	0	

801D	0	0	0	0	0	0	0	0	
801E	0	0	0	0	0	0	0	0	
801F	0	0	0	0	0	0	0	0	
8020	0	0	0	0	0	0	0	0	
8021	0	0	0	0	0	0	0	0	
8022	0	0	0	0	0	0	0	0	Fiber distance is 300 meters
8023	0	0	0	1	1	1	1	0	
8024	0	0	0	0	0	0	0	1	Fiber type is Multi-mode generic
8025	0	0	0	0	0	0	0	0	
8026	0	0	0	0	0	0	0	1	Center optical wavelength is 1310nm
8027	1	1	1	1	1	1	1	1	
8028	1	0	1	1	1	0	0	0	
8029	0	0	0	0	0	0	0	0	*Channel 1 wavelength – not applicable*
802A	0	0	0	0	0	0	0	0	
802B	0	0	0	0	0	0	0	0	
802C	0	0	0	0	0	0	0	0	*Channel 2 wavelength – not applicable*
802D	0	0	0	0	0	0	0	0	
802E	0	0	0	0	0	0	0	0	
802F	0	0	0	0	0	0	0	0	*Channel 3 wavelength – not applicable*
8030	0	0	0	0	0	0	0	0	
8031	0	0	0	0	0	0	0	0	
8032	0	0	0	0	0	0	0	0	Package Identifier OUI for X2
8033	1	0	1	0	0	0	0	0	
8034	1	0	0	1	1	0	0	0	
8035	0	0	1	0	0	1	1	0	
8036	0	0	0	0	0	0	1	1	Big Bear OUI is 00-0F-3F Model Number is 00010 Revision Number starts at 00
8037	1	1	0	0	0	0	1	1	
8038	1	1	1	1	0	0	0	0	
8039	0	0	0	0	0	0	0	0	
803A	0	1	0	0	0	0	1	0	B
803B	0	1	0	0	1	0	0	1	I
803C	0	1	0	0	0	1	1	1	G
803D	0	0	1	0	0	0	0	0	
803E	0	1	0	0	0	0	1	0	B
803F	0	1	0	0	0	1	0	1	E
8040	0	1	0	0	0	0	0	1	A
8041	0	1	0	1	0	0	1	0	R
8042	0	0	1	0	0	0	0	0	
8043	0	1	0	0	1	1	1	0	N
8044	0	1	0	1	0	1	0	0	T
8045	0	1	0	1	0	1	1	1	W
8046	0	1	0	1	0	0	1	0	R
8047	0	1	0	0	1	0	1	1	K

8048	0	1	0	1	0	0	1	1	S
8049	0	0	1	0	0	0	0	0	blank
804A	0	1	0	0	0	0	1	0	B
804B	0	1	0	0	0	0	1	0	B
804C	0	1	0	1	0	1	0	0	T
804D	0	1	0	1	0	0	1	0	R
804E	0	0	1	1	0	0	0	1	1
804F	0	0	1	1	0	0	0	0	0
8050	0	0	1	1	0	0	1	1	3
8051	0	0	1	1	0	0	0	1	1
8052	0	0	1	1	0	0	0	0	0
8053	0	0	1	0	1	1	0	1	dash
8054	0	1	0	1	1	0	0	0	X
8055	0	0	1	1	0	0	0	1	1
8056	0	0	1	0	0	0	0	0	blank
8057	0	0	1	0	0	0	0	0	blank
8058	0	0	1	0	0	0	0	0	blank
8059	0	0	1	0	0	0	0	0	blank
805A	0	0	1	1	0	0	0	0	Vendor Revision (ASCII « 01 »)
805B	0	0	1	1	0	0	0	1	
805C – 806B									Vendor Serial Number
806C	0	0	1	1	0	0	1	0	Vendor Date Code : Year in 1000 (2)
806D	0	0	1	1	0	0	0	0	Vendor Date Code : Year in 100 (0)
806E									Vendor Date Code : Year in 10 (various)
806F									Vendor Date Code : Year in 1 (various)
8070									Vendor Date Code : Month in 10 (various)
8071									Vendor Date Code : Month in 1 (various)
8072									Vendor Date Code : Day in 10 (various)
8073									Vendor Date Code : Day in 1 (various)
8074									Lot Code in 10
8075									Lot Code in 1
8076	0	0	0	0	0	0	0	0	Current required at 5V is zero
8077	0	0	0	1	0	0	0	0	Current required at 3.3V is 1200mA (60% of 2A)
8078	0	0	0	0	1	0	0	0	Current required at APS is 1000mA (50% of 2A)
8079	0	0	0	0	1	0	0	0	APS Voltage is 1.25V
807A	1	1	0	0	0	0	0	1	Big Bear supports DOM Laser Bias Factor is 2uA (Bit 4 = 0)
807B									Reserved
807C									Reserved
807D									Checksum
807E to 80AD									CUSTOMER WRITABLE AREA
80AE to 8106									BIG BEAR SPECIFIC AREA
8017 to 8FFF									BIG BEAR SPECIFIC AREA EXTENDED

LASI Control and Status (0x9000 Series)

Register 1.36864 (0x9000) - RX_ALARM Control

Bit	Name	Description	R/W	Default
1.36864.15:11	Reserved		RO	0
1.36864.10	Vendor Specific			
1.36864.9	WIS Local Fault Enable	NOT SUPPORTED		
1.36864.8:7	Vendor Specific			
1.36864.6	Vendor Specific			
1.36864.5	Receive Optical Power Fault Enable	1 = Receive Optical Power Fault Enable 0 = Receive Optical Power Fault Disable	RW	1
1.36864.4	PMA/PMD Local Fault Enable	1 = PMA/PMD Local Fault Enable 0 = PMA/PMD Local Fault Disable	RW	1
1.36864.3	PCS Receive Local Fault Enable	1 = PCS Receiver Local Fault Enable 0 = PCS Receiver Local Fault Disable	RW	1
1.36864.2	Vendor Specific			
1.36864.1	Vendor Specific			
1.36864.0	PHY XS Receive Local Fault Enable	1 = PHY XS Receive Local Fault Enable 0 = PHY XS Receive Local Fault Disable	RW	1

NOTE: The contents of register 0x9003 shall be AND'ed with the contents of register 0x9000 prior to application of the OR function that generates the RX_ALARM.

Register 1.36865 (0x9001) - TX_ALARM Control

Bit	Name	Description	R/W	Default
1.36865.15:11	Reserved		RO	
1.36865.10	Vendor Specific			
1.36865.9	*Laser Bias Current Fault Enable*	*1 = Laser Bias Current Fault Enable* *0 = Laser Bias Current Fault Disable*		*1*
1.36865.8	*Laser Temperature Fault Enable*	*1 = Laser Temperature Fault Enable* *0 = Laser Temperature Fault Disable* *NOT SUPPORTED*		*0*
1.36865.7	*Laser Output Fault Enable*	*1 = Laser Output Fault Enable* *0 = Laser Output Fault Disable*		*1*
1.36865.6	Transmitter Fault Enable	1 = Transmitter Fault Enable 0 = Transmitter Fault Disable	RW	1
1.36865.5	Vendor Specific			
1.36865.4	*PMA/PMD Transmitter Local Fault Enable*	*1 = enable* *0 = disable*		*1*
1.36865.3	PCS Transmit Local Fault Enable	1 = enable 0 = disable	RW	1
1.36865.2	Vendor Specific			
1.36865.1	Vendor Specific			
1.36865.0	PHY_XSTransmit Local Fault Enable	1 = enable 0 = disable	RW	1

Note 1: The contents of register 0x9004 shall be AND'ed with the contents of register 0x9001 prior to application of the OR function that generates the RX_ALARM.

Register 1.36866 (0x9002) - LASI Control

Bit	Name	Description	R/W	Default
1.36866.15:8	Reserved		RO	0
1.36866.7	Vendor specific			
1.36866.6	Vendor specific	TBD		
1.36866.5	Vendor specific	TBD		
1.36866.4	Vendor specific	TBD		
1.36866.3	Vendor specific	TBD		
1.36866.2	RX_ALARM Enable	1 = enable 0 = disable	RW	1
1.36866.1	TX_ALARM Enable	1 = enable 0 = disable	RW	1
1.36866.0	LS_ALARM Enable	1 = enable 0 = disable	RW	1

Register 1.36867 (0x9003) - RX_ALARM Status

Bit	Name	Description	R/W	Default
1.36867.15:11	Reserved		RO	0
1.36867.10	Vendor Specific			
1.36867.9	*WIS Local Fault*	*Not Supported*	*RO/LH*	
1.36867.8:7	Vendor Specific			
1.36867.6	Vendor Specific			
1.36867.5	*Receive Optical Power Fault*	*1 = Alarm Active (NOTE: this is non-latching)* *0 = Normal*	*RO*	*0*
1.36867.4	*PMA/PMD Local Fault*	*1 = Alarm Active (Latching)* *0 = Normal* *(Mirror of register 1.8.10 which is the PMA/PMD Receive Fault)*	*RO/LH*	*0*
1.36867.3	PCS Receive Local Fault	1 = Alarm Active 0 = Normal (Mirror of register 3.8.10 which is a PCS receive fault)	RO/LH	0
1.36867.2	Vendor Specific			
1.36867.1	Vendor Specific			
1.36867.0	PHY XS Receive Local Fault	1 = Alarm Active (Latching) 0 = Normal (This is a mirror of register 4.8.10)	RO/LH	0

Register 1.36868 (0x9004) - TX_ALARM Status

Bit	Name	Description	R/W	Default
1.36868.15:11	Reserved		RO	
1.36868.10	Vendor Specific			
1.36868.9	*Laser Bias Current Fault*	*1 = Alarm Active (Note: this is non-latching)* *0 = Normal*	*RO*	*0*
1.36868.8	*Laser Temperature Fault*	*1 = Alarm Active (Note: this is non-latching)* *0 = Normal* *NOT SUPPORTED*	*RO*	*0*
1.36868.7	*Laser Output Fault*	*1 = Alarm Active (Note: this is non-latching)* *0 = Normal*	*RO*	*0*
1.36868.6	Transmitter Fault	1 = Alarm Active 0 = Normal	RO/LH	0
1.36868.5	Vendor Specific			
1.36868.4	*PMA/PMD Transmitter Local Fault*	*1 = Alarm Active (latching)* *0 = Normal* *(Mirror of register 1.8.11)*	*O/RO/LH*	*0*

1.36868.3	PCS Transmit Local Fault	1 = Alarm Active (latching) 0 = Normal (This is a mirror of register 3.8.11)	RO/LH	0
1.36868.2	Vendor Specific			
1.36868.1	Vendor Specific			
1.36868.0	PHY XS Transmit Local Fault	1 = Alarm active (latching) 0 = Normal (This is a mirror of register 4.8.11)	RO/LH	0

Register 1.36869 (0x9005) - LASI Status

Bit	Name	Description	R/W	Default
1.36869.15:8	Reserved		RO	0
1.36869.7	Vendor specific			
1.36869.6	Vendor specific			
1.36869.5	Vendor specific			
1.36869.4	Vendor specific			
1.36869.3	Vendor specific			
1.36869.2	RX_ALARM	1 = Alarm Active 0 = normal (Note 1)	RO	0
1.36869.1	TX_ALARM	1 = Alarm Active 0 = normal (Note 2)	RO	0
1.36869.0	LS_ALARM	1 = Alarm Active 0 = normal	LH	0

NOTES:

1. The assertion of RX_ALARM (in LASI) indicates that a fault has occurred in the receive path of the X2 module. RX_ALARM is an OR of the bits in register 9003. (The contents of register 0x9003 are AND'ed with the contents of register 0x9000 prior to application of the OR function that generates the RX_ALARM)
2. The assertion of TX_ALARM (in LASI) indicates that a fault has occurred in the transmit path of the X2 module. TX_ALARM is an OR of the bits in register 9004. (The contents of register 0x9004 are AND'ed with the contents of register 0x9001 prior to application of the OR function that generates the TX_ALARM)

LS_ALARM

The LS_ALARM (bit 0 in the LASI Status Byte) is the logical 'AND' of the signals in the following Table (which is same as Table 20 in the XENPAK MSA).

Signal	Source
Global PMD Signal OK	1.10.0
PCS Block Lock	3.32.0
PHY XS Lane Alignment	4.24.12

Digital Optical Monitoring

Per the XENPAK MSA the Digital Optical Monitoring (DOM) registers are a 256 Byte register space that is accessible via the MDIO interface. The DOM provides for measurements and associated alarms of transceiver temperature, receive optical power, laser output power, and laser bias current.

The Big Bear LRM-LR transponder supports three key optical values in the DOM:

- Laser Bias Current
- Laser Output Power
- Receive Optical Power

The Big Bear LRM-LR transponder supports high and low alarm flags for these three parameters but does not support warning flags.

DOM Register (Hex)	Register Name	Big Bear LRM-LR
0xA000 – 0xA027	Alarm and Warning Thresholds	Alarm Thresholds are supported but Warning Thresholds are not Supported
0xA028 – 0xA047	Vendor Specific	None
0xA048 – 0xA05F	CWDM Alarm and Warning Thresholds	NOT APPLICABLE
0xA060 – 0xA061	Transceiver Temperature	NOT SUPPORTED
0xA062 – 0xA063	Reserved	
0xA064 – 0xA065	Laser Bias Current	SUPPORTED
0xA066 – 0xA067	Laser Output Power	SUPPORTED
0xA068 – 0xA069	Receive Optical Power	SUPPORTED
0xA06A – 0xA06D	Reserved	
0xA06E	Optional Status Bits	None
0xA06F	DOM Capability Extended	None
0xA070 – 0A077	Alarm and Warning Flags	None
0xA078 – 0xA0BF	Vendor Specific	None
0xA0C0 – 0xA0FF	CWDM Digital Optical Monitoring Interface	NOT APPLICABLE
0xA100	Optional DOM Control / Status	None

Table 19: Alarm Thresholds (Subject to Change)

Register	Item	Threshold for Alarm
A010-A011	Laser Bias High Alarm	> 1.5 times beginning of life bias current measured at 70C
A012-A013	Laser Bias Low Alarm	< 0.5 times beginning of life bias current measured at 0C
A018-A019	Laser Output Average Power High Alarm	> 2dBm (±1.5dB)
A01A-A01B	Laser Output Average Power Low Alarm	< -8dBm (±1.5dB)
A020-A021	Receive Optical Power High Alarm	> 1.5dBm (±1dB)
A022-A023	Receive Optical Power Low Alarm	< -15.5dBm (±1.1dB)

Transceiver Temperature

Not currently Supported

Laser Bias Current (0xA064 – 0xA065)

Per the XENPAK MSA this is the measured laser bias current in μA. The current is represented as a 16 bit unsigned integer with the current defined as the full 16 bit value (0-65535) with LSB equal to 2 μA. (Note that this LSB value is indicated by a 0 in bit 4 of register 0x807A (Digital Monitoring Capability).

Laser Output Power (0xA066 – 0xA067)

Per the XENPAK MSA this is the measured laser output power in mW. For the LRM-LR transponder this is the power launched into a MMF fiber. The power is represented as a 16 bit unsigned integer with the power defined as the full 16 bit value (0-65535) with LSB equal to 0.1 μW.

Receive Optical Power (0xA068 – 0xA069)

Per the XENPAK MSA this is the measured receive optical power in mW. The power is represented as a 16 bit unsigned integer with the power defined as the full 16 bit value (0-65535) with LSB equal to 0.1 μW

Device 3 PCS Registers

Dev	PCS Register (Decimal)	PCS Register (Hex)	Register Name
3	0	0000	PCS Control 1
3	1	0001	PCS Status 1
3	2-3	0002-0003	PCS Device Identifier
3	4	0004	PCS Speed Ability
3	5-6	0005-0006	PCS Devices in Package
3	7	0007	10G PCS Control 2
3	8	0008	10G PCS Status 2
3	9-13	0009 – 000D	Reserved
3	14-15	000E – 000F	PCS Package Identifier
3	16 – 23	0010 - 0017	Reserved
3	24	0018	10GBASE-X PCS Status
3	25	0019	10GBASE-X PCS test control
3	26-31	001A – 001F	Reserved
3	32	0020	10GBASE-R PCS status 1
3	33	0021	10GBASE-R PCS status 2
3	34 - 37	0022 - 0025	10GBASE-R PCS test pattern seed A
3	38 – 41	0026 - 0029	10GBASE-R PCS test pattern seed B
3	42	002A	10GBASE-R PCS test pattern error control
3	43	002B	10GBASE-R PCS test pattern error counter
3	44 – 32767	002C – 7FFF	Reserved
3	32768 - 65535	8000 - FFFF	Vendor Specific

Register 3.0 (0x0000) – PCS Control 1

Bit	Name	Description	R/W	Default
3.0.15	Reset	1= PCS Reset 0 = Normal Operation	RW (SC)	0
3.0.14	Loopback	1 = Enable PCS Loopback Mode 0 = Disable PSC Loopback Mode	RW	0
3.0.13	Speed Selection	1 = Operation at 10Gb/s and above 0 = Unspecified	RW	1
3.0.12	Reserved	Value always 0, writes ignored	RW	0
3.0.11	Low Power	1 = Low Power Mode 0 = Normal Operation	RW	0
3.0.10:7	Reserved	Value always 0, writes ignored	RW	
3.0.6	Speed Selection	1, Operation at 10Gb/s and above	RW	1
3.0.5:2	Speed Selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = Reserved 0 0 0 0 = 10Gb/s	RW	0 0 0 0
3.0.1:0	Reserved	Value always 0, writes ignored		0

Register 3.1 (0x0001) – PCS Status 1

Bit	Name	Description	R/W	Default
3.1.15:8	Reserved	Ignore when read	RO	0
3.1.7	Fault	1 = Fault Condition Detected 0 = No Fault Condition Detected	RO	0
3.1.6:3	Reserved	Ignore when read	RO	0
3.1.2	PCS Receive link status	1 = PCS receive link up 0 = PCS receive link down	RO (Latch Low)	1
3.1.1	Low power ability	1 = PCS supports low power mode	RO	1
3.1.0	Reserved	Ignore when read	RO	

Register 3.2 – 3.3 (0x0002 – 0x0003) – PCS Device Identifier

These registers contain the Identifier of the PCS Device used in the transponder.

Register 3.4 (0x0004) – PCS Speed Ability

Bit	Name	Description	R/W	Default
3.4.15:1	Reserved	Ignore when read	RO	0
3.4.0	10G Capable	1, PCS is capable of operating at 10Gb/s	RO	1

Register 3.5 – 3.6 (0x0005 – 0x0006) – PCS Devices in Package

These are mirrors of Registers 1.5 – 1.6

Register 3.7 (0x0007) – PCS Control 2

Bit	Name	Description	R/W	Default
3.7.15:1	Reserved	Value always 0, writes ignored	RW	0
3.7.0	PCS Type Selection	1 0 1 1 Reserved 1 0 Select 10GBASE-W PCS Type 0 1 Select 10GBASE-X PCS Type 0 0 Select 10GBASE-R PCS Type	RW	0 0

Register 3.8 (0x0008) – PCS Status 2

Bit	Name	Description	R/W	Default
3.8.15:14	Device Present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO	1 0
3.8.13:12	Reserved	Ignore when read	RO	0
3.8.11	Transmit Fault	1 = Fault condition on the transmit path 0 = No Fault condition on the transmit path Transmit Fault = inverse lsync (3:0)	RO / LH	0
3.8.10	Receive Fault	1 = Fault condition on the receive path 0 = No Fault condition on the receive path Receive Fault = inverse block_lock	RO /LH	0
3.8.9:3	Reserved	Ignore when read	RO	0
3.8.2	10GBASE-W capable	0, PCS is not able to support 10GBASE-W PCS type	RO	0
3.8.1	10GBASE-X capable	0, PCS is not able to support 10GBASE-X PCS type	RO	0
3.8.0	10GBASE-R capable	1, PCS is able to support 10GBASE-R PCS type	RO	1

Register 3.32 (0x0020) – 10GBASE-R PCS Status 1

Bit	Name	Description	R/W	Default
3.32.15:13	Reserved	Ignore when read	RO	
3.32.12	10GBASE-R receive link status	1 = 10GBASE-R PCS receive link up 0 = 10GBASE-R PCS receive link down PCS receive link up = block_lock AND inv high_BER	RO	1
3.32.11:3	Reserved	Ignore when read	RO	
3.32.2	PRBS31 pattern testing ability	1, PCS is able to support PRBS31 pattern testing	RO	1
3.32.1	10GBASE-R PCS High BER	1 = 10GBASE-R PCS reporting a high BER 0 = 10GBASE-R PCS not reporting a high BER	RO	0
3.32.0	10GBASE-R PCS block lock	1 = 10GBASE-R PCS locked to received blocks 0 = 10GBASE-R PCS not locked to received blocks	RO	1

Register 3.33 (0x0021) – 10GBASE-R PCS Status 2

Bit	Name	Description	R/W	Default
3.33.15	Latched block lock	1 = 10GBASE-R PCS has block lock 0 = 10GBASE-R PCS does not have block lock	RO/LL	1
3.33.14	Latched high BER	1 = 10GBASE-R PCS has reported a high BER 0 = 10GBASE-R PCS has not reported a high BER	RO/LH	0
3.33.13:8	BER	BER Counter	RO/NR	
3.33.7:0	Errored Blocks	Errored blocks counter	RO/NR	

Register 3.34 – 3.37 (0x0022 – 0x0025) – 10GBASE-R PCS test pattern seed A

Bit	Name	Description	R/W	Default
3.37.15:10	Reserved	Value always 0, writes ignored	RW	
3.37.9:0	Test pattern seed A 3	Test pattern seed A bits 48 – 57	RW	
3.36.15:0	Test pattern seed A 2	Test pattern seed A bits 32 - 47	RW	
3.35.15:0	Test pattern seed A 1	Test pattern seed A bits 16 - 31	RW	
3.34.15:0	Test pattern seed A 0	Test pattern seed A bits 0 - 15	RW	

Register 3.38 – 3.41 (0x0026 – 0x0029) – 10GBASE-R PCS test pattern seed B

Bit	Name	Description	R/W	Default
3.41.15:10	Reserved	Value always 0, writes ignored	RW	0
3.41.9:0	Test pattern seed B 3	Test pattern seed B bits 48 – 57	RW	
3.40.15:0	Test pattern seed B 2	Test pattern seed B bits 32 - 47	RW	
3.39.15:0	Test pattern seed B 1	Test pattern seed B bits 16 - 31	RW	
3.38.15:0	Test pattern seed B 0	Test pattern seed B bits 0 - 15	RW	

Register 3.42 (0x002A) – 10GBASE-R PCS Test Pattern Control

Bit	Name	Description	R/W	Default
3.42.15:6	Reserved	Value always 0, writes ignored	RW	0
3.42.5	PRBS31 receive test pattern enable	1 = Enable PRBS31 test pattern mode on the receive path 0 = Disable PRBS31 test pattern mode on the receive path	RW	
3.42.4	PRBS31 transmit test pattern enable	1 = Enable PRBS31 test pattern mode on the transmit path 0 = Disable PRBS31 test pattern mode on the transmit path	RW	
3.42.3	Transmit test pattern enable	1 = enable test pattern 0 = disable test pattern	RW	
3.42.2	Receive test pattern enable	1 = enable test pattern 0 = disable test pattern	RW	
3.42.1	Test pattern select	1 = Square wave test pattern 0 = Pseudo random test pattern	RW	
3.42.0	Data pattern select	1 = Zeros data pattern 0 = LF data pattern	RW	

Register 3.43 (0x002B) – 10GBASE-R PCS Test Pattern Error Counter

Bit	Name	Description	R/W	Default
3.43.15:0	Test pattern error counter	Error Counter LSB = Bit 0, MSB = bit 15	RO	

Device 4 PHY XS Registers

Dev	PHY XS Register (Decimal)	PHY XS Register (Hex)	Register Name
4	0	0000	PHY XS Control 1
4	1	0001	PHY XS Status 1
4	2-3	0002 – 0003	PHY XS Device Identifier
4	4	0004	PHY XS Speed Ability
4	5-6	0005 – 0006	PHY XS Devices in Package
4	7	0007	Reserved
4	8	0008	PHY XS Status 2
4	9 – 13	0009 – 000D	Reserved
4	14-15	000E – 000F	PHY XS Package Identifier
4	24	0018	10G PHY XGXS Lane Status
4	25	0019	10G PHY XGXS Test Control
4	26 – 32767	001A – 7FFF	Reserved
4	32768 – 65535	8000 – FFFF	Vendor Specific

Register 4.0 (0x0000) – PHY XS Control 1

Bit	Name	Description	R/W	Default
4.0.15	Reset	1= PHY XS Reset 0 = Normal Operation	RW (SC)	0
4.0.14	Loopback	1 = Enable PHY XS (XGXS) Network Loopback Mode 0 = Disable PHY XS (XGXS) Network Loopback Mode	RW	0
4.0.13	Speed Selection	1, Operation at 10Gb/s and above	RW	1
4.0.12	Reserved	Value always 0, writes ignored	RW	
4.0.11	Low Power	1 = Low Power Mode 0 = Normal Operation	RW	0
4.0.10:7	Reserved	Value always 0, writes ignored	RW	0
4.0.6	Speed Selection	1, Operation at 10Gb/s and above	RW	1
4.0.5:2	Speed Selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = Reserved 0 0 0 0 = 10Gb/s	RW	0 0 0 0
4.0.1:0	Reserved	Value always 0, writes ignored	RW	0

Register 4.1 (0x0001) – PHY XS Status 1

Bit	Name	Description	R/W	Default
4.1.15:8	Reserved	Ignore when read	RO	0
4.1.7	Fault	1 = Fault Condition Detected 0 = No Fault Condition Detected	RO	0
4.1.6:3	Reserved	Ignore when read	RO	0
4.1.2	PHY XS Receive link status	1 = PHY XS receive link up 0 = PHY XS receive link down Latched low version of register 4.24.12.	RO (Latch Low)	1
4.1.1	Low power ability	1, PHY XS supports low power mode	RO	0
4.1.0	Reserved	Ignore when read	RO	0

Register 4.2 – 4.3 (0x0002 – 0x0003) – PHY XS Device Identifier

These registers contain the identifier of the PHY XS device used in the transponder.

Register 4.4 (0x0004) – PHY XS Speed Ability

Bit	Name	Description	R/W	Default
4.4.15:1	Reserved	Ignore when read	RO	0
4.4.0	10G Capable	1, PHY XS is capable of operating at 10Gb/s	RO	1

Register 4.5 – 4.6 (0x0005 – 0x0006) – PHY XS Devices In Package

These are mirrors of Registers 1.5 – 1.6

Register 4.8 (0x0008) – PHY XS Status 2

Bit	Name	Description	R/W	Default
4.8.15:14	Device Present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO	1 0
4.8.13:12	Reserved	Ignore when read	RO	0
4.8.11	Transmit Fault	1 = Fault condition on the transmit path of PHY XS 0 = No Fault condition on the transmit path of PHY XS	RO / LH	0
4.8.10	Receive Fault	1 = Fault condition on the receive path of PHY XS 0 = No Fault condition on the receive path of PHY XS	RO /LH	0
4.8.9:0	Reserved	Ignore when read	RO	0

Register 4.14 – 4.15 (0x000E – 0x000F) – PHY XS Package Identifier

These are mirrors of Registers 1.32818 – 1.32821

Register 4.24 (0x0018) – 10G PHY XS Lane Status

Bit	Name	Description	R/W	Default
4.24.15:13	Reserved	Ignore when read	RO	0
4.24.12	PHY XGXS Lane Alignment	1 = PHY XGXS transmit lanes aligned 0 = PHY XGXS transmit lanes not aligned	RO	1
4.24.11	Pattern testing ability	1 = PHY XGXS is able to generate test patterns 0 = PHY XGXS is not able to generate test patterns	RO	1
4.24.10	PHY XGXS Loopback Capability	1 = PHY XGXS is able to perform loopback 0 = PHY XGXS is not able to perform loopback	RO	1
4.24.9:4	Reserved	Ignore when read	RO	0
4.24.3	Lane 3 Sync	1 = Lane 3 is synchronized 0 = Lane 3 is not synchronized	RO	1
4.24.3	Lane 2 Sync	1 = Lane 2 is synchronized 0 = Lane 2 is not synchronized	RO	1
4.24.3	Lane 1 Sync	1 = Lane 1 is synchronized 0 = Lane 1 is not synchronized	RO	1
4.24.3	Lane 0 Sync	1 = Lane 0 is synchronized 0 = Lane 0 is not synchronized	RO	1

Register 4.25 (0x0019) – 10G PHY XS Test Control

Bit	Name	Description	R/W	Default
4.25.15:3	Reserved	Value always 0, writes	RW	0
4.24.2	Receive test pattern enable	1 = Receive test pattern enabled 0 = Receive test pattern disabled	RW	0
4.25.1:0	Test pattern select	1 0 1 1 = Reserved 1 0 = Mixed frequency test pattern 0 1 = Low frequency test pattern 0 0 = High frequency test pattern	RW	

Revision History

Revision	Date	Description
0.1	1/13/05	▪ Draft of document layout.
0.2	2/15/05	▪ Incorporated feedback from engineering and marketing within BBN
0.3c	5/27/05	▪ Minor text revisions.
0.5	8/2/2005	▪ Clarifying LRM optical specifications per IEEE802.3aq draft 2.2 ▪ Adding three DOM parameters and related high and low alarms ▪ Incorporated concise form of NVRAM table. ▪ Corrected OUI registers
0.5a	8/3/2005	▪ Corrected alarm latching and minor text edits.

Additional Information

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